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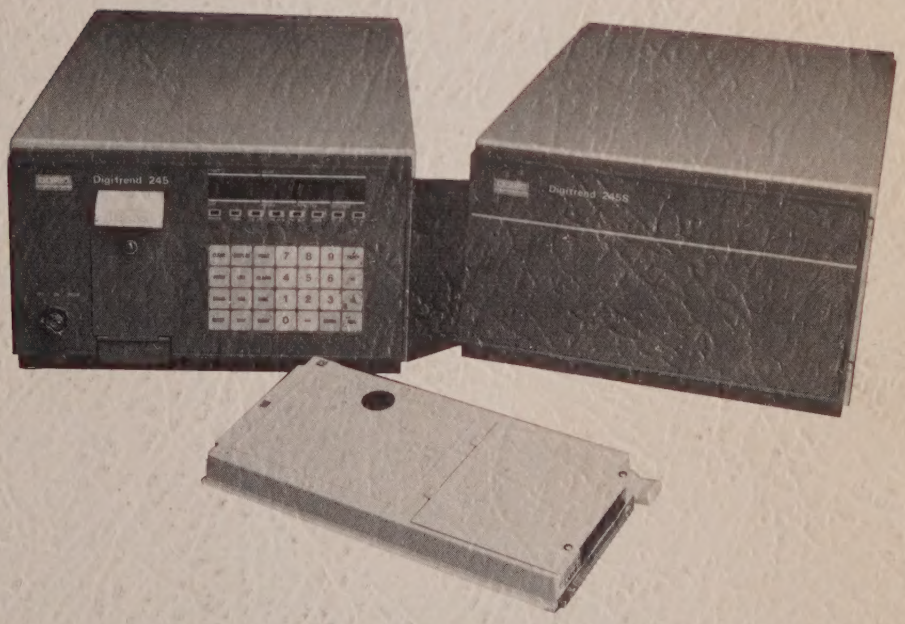
Digitrend® 245

DATA LOGGER



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MAINTENANCE MANUAL

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2. Commencing with the date of shipn of each instrument to the original purchaser, Doric Scientific UNCONDITIONALLY WARRANTS that each unit shall remain free from defect in parts, materials and workmanship for a period of TWO YEARS.

In the event any instrument fails to meet the terms of this warranty, Doric Scientific agrees to provide corrective action. Refer to Warranty Claim (below) for proper procedure.

The warranties herein shall not obligate Doric Scientific in any manner whatsoever with respect to, and shall not be applicable to, any defects which after an inspection by Doric Scientific are not to Doric Scientific's reasonable satisfaction demonstrably the result of defective parts, materials or workmanship. We are not liable for consequential damages.

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Doric Scientific certifies that the instrument was thoroughly tested and inspected and found to meet its published specifications when shipped from the factory. Doric Scientific further certifies that its calibration measurements are traceable to NBS.

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1

Calibration Procedures

1.1 INTRODUCTION TO CALIBRATION

The design of the Digitrend® 245 data logger incorporates digital data comparison that enables field calibration of a FEM (Front End Module) without the need for any potentiometer adjustments.

With a FEM receiving a calibrated voltage source input, the source input numerical value is entered via a calibration command entry. The data logger computes a ratio by comparing the entered number with the actual reading. This ratio is stored in memory as a calibration constant.

Two types of calibration constants are stored in memory. These are the zero (offset) and +full scale (gain) calibration constants. The zero calibration constant is subtracted from the reading to set the zero reference point. The reading is then multiplied by the +full scale calibration constant to normalize the slope from the zero reference point.

Calibration is performed on one selected data point of a FEM using the linear voltage functions. Solid State and Reed FEMs are calibrated to store the correct calibration constants for point functions 2, 3, 4, and 5. Calibration constants for Current and High Voltage FEMs are determined on point functions 4 and 6 respectively. Once a FEM has been calibrated on the linear voltage functions, the FEM is calibrated for all data points and all point functions.

An RTD type FEM calibrates itself using an onboard precision resistor (0.01% tolerance). No field calibration is required for this type of FEM because the resistor value is read periodically and the calibration constant is updated accordingly.

1.2 SOLID-STATE AND REED RELAY FEM CALIBRATION

Test Equipment Required:

Precision voltage (millivolt/volt) calibrator with integral digital readout: resolution, 1 uV; accuracy $\pm$ .01% ($\pm$ 2 uV).

1.2.1 Preliminary Set-up

a. Apply power to the calibrator and allow warm-up time in accordance with the calibrator operating manual.

b. Adjust calibrator output to 0 (zero) volts.

c. Remove power from the data logger system.

d. Remove the FEM module to be calibrated from the card cage.

e. Set the module on a flat work area with the large bare aluminum plate on the module facing downwards. Remove the cover plate to access the input terminals.

f. Buss all positive (+) inputs together and connect to the calibrator positive (+) output.

g. Buss all negative (-) inputs together and connect to the calibrator negative (-) output.

h. Replace the cover over the input terminals.

i. Return the FEM to the card cage slot in which it will finally be installed.

j. Fasten the grounding lug at the bottom of the FEM module.

k. Apply power to the data logger system, placing the mainframe keyswitch in PRGM. Allow 5 minutes warm-up time before proceeding to 1.2.2.a.

1.2.2 Calibration

a. Place the mainframe keyswitch in PRGM if not already done.

Calibration is performed on each of these point functions for Solid-state and Reed FEMs:

Function 1 or 2*
Function 3
Function 4
Function 5

* Use Function 1 if configuration switch #1 is set CLOSED/ON (low sensitivity). Use Function 2 if configuration switch #1 is set OPEN/OFF (high sensitivity). Refer to the Operator's Manual (4.6.2) for more information on assigning function numbers to data points.

TABLE 1-1. FEM POINTS VERSUS SLOT LOCATION AND FEM NUMBER

FEM SLOT	FEM NUMBER	FIRST POINT	LAST POINT
MAINFRAME			
5	1	1	20
4	2	21	40
3	3	41	60
2	4	61	80
1	5	81	100
SAT. #1			
5	6	101	120
4	7	121	140
3	8	141	160
2	9	161	180
1	10	181	200
SAT. #2			
5	11	201	220
4	12	221	240
3	13	241	260
2	14	261	280
1	15	281	300
SAT. #3			
5	16	301	320
4	17	321	340
3	18	341	360
2	19	361	380
1	20	381	400
SAT. #4			
5	21	401	520
4	22	421	540
3	23	441	560
2	24	461	580
1	25	481	500

b. Assign one of the above linear voltage functions to all points within the FEM:

[CLEAR] [PRGM] [POINT] [first point no.] [-] [last point no.] [FUNC]

[function no.] [RUN]

Specify the first and last points of the FEM according to the unit it belongs to and its slot location. Refer to Table 1-1.

c. Adjust calibrator output to 0.000 mV (use lowest range).

d. Wait at least 10 seconds to allow all FEM channels to be read.

e. Log the points within the FEM:

[CLEAR] [LOG] [POINT] [first point no.] [-] [last point no.] [RUN]

f. Examine the log and determine which point number has its value closest to mid-point of the voltage scatter.

g. Access the point number determined to be at mid-point for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

NOTE

Do not leave the Reed FEM in the calibration mode for more time than is necessary to perform calibration (approx. 20 seconds). Thermal offsets produced by the relay coil may introduce an error in calibration when time in calibration is in excess of 20 seconds.

h. Initiate the zero calibration constant computation by entering the following command:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

After entering the command, the display will update with the correct reading of the input.

i. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

j. Adjust the calibrator output to the +full scale value of the function being calibrated. Refer to Table 1-2 below.

TABLE 1-2. CALIBRATION CHART FOR SOLID-STATE AND REED FEMS

FUNCTION	CALIBRATION VOLTAGE (+Full Scale)	KEYBOARD ENTRY*	COMMENT
1	+9.9900 mV	19980	Keyboard entry is 20% of input.
2	+20.000 mV	20000	———
3	+80.000 mV	40000	Keyboard entry is 50% of input.
4	+400.00 mV	40000	———
5	+2.0000 V	20000	———

* For calibration of low sensitivity instruments, delete the last zero of the keyboard entries shown.

k. Wait at least 10 seconds to allow all FEM channels to be read.

l. Access the point used previously for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

m. Initiate the +full scale calibration constant computation by using this command (enter the exact value of the calibrator source):

[CLEAR] [PRGM] [CALIB] [+full scale value] [RUN]

After entering the command, the display will update with the correct reading.

NOTE

You must enter 20% of the +full scale value when calibrating Function 1 for the +full scale calibration constant. You must enter 50% of the +full scale value when calibrating Function 3 for the +full scale calibration constant. Refer to Table 1-2.

n. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

o. Repeat steps 1.2.2.b through 1.2.2.n for the remaining linear voltage functions to be calibrated.

p. Now list the calibrations constants for that FEM by entering this command:

[CLEAR] [LIST] [1] [CALIB] [fem no.] [RUN]

This command will give you a printout of the FEM's calibration constants. These constants will be most useful if you have to move this FEM to another slot or another Digitrend 245 data logger system, or if you decide to use this FEM in a remote application. Refer to 1.5.

SOLID-STATE AND REED FEM CALIBRATION COMPLETED

1.3 CURRENT FEM CALIBRATION

Test Equipment Required:

Precision current calibrator with integral digital readout: resolution, 1 uA; accuracy $\pm$ .01% ($\pm$ 2 uA).

1.3.1 Preliminary Set-up

a. Apply power to the calibrator and allow warm-up time in accordance with the calibrator operating manual.

b. Adjust calibrator output to 0 (zero) milliamps.

c. Remove power from the data logger system.

d. Remove the FEM module to be calibrated from the card cage.

e. Set the module on a flat work area with the large bare aluminum plate on the module facing downwards. Remove the cover plate to access the input terminals.

f. Buss all terminals in series: connect the positive (+) terminal of the first point to the calibrator positive (+) output. Connect the negative (-) terminal of the first point to the positive terminal of the second point. Connect the negative (-) terminal of second point connected to the positive terminal of the third point, continuing on through all points in sequence until the negative terminal of the twentieth point is reached. Connect the calibrator negative output to the negative terminal of the twentieth point.

g. Replace the cover over the input terminals.

h. Return the FEM to the card cage slot in which it will finally be installed.

i. Fasten the grounding lug at the bottom of the FEM module.

j. Apply power to the data logger system, placing the mainframe keyswitch in PRGM. Allow 5 minutes warm-up time before proceeding to 1.3.2.a.

1.3.2 Calibration

a. Place the mainframe keyswitch in PRGM if not already done.

b. Assign Function 4 to all points within the FEM:

[CLEAR] [PRGM] [POINT] [first point no.] [-] [last point no.]

[FUNC] [4] [RUN]

Specify the first and last points of the FEM according to its slot location. Refer to Table 1-1.

c. Adjust calibrator output to 0.0 mA.

d. Wait at least 10 seconds to allow all FEM channels to be read.

e. Log the points within the FEM:

[CLEAR] [LOG] [POINT] [first point no.] [-] [last point no.] [RUN]

f. Examine the log and determine which point number has its value closest to mid-point of the voltage scatter.

g. Access the point number determined to be at mid-point for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

NOTE

Do not leave the Current FEM in the calibration mode for more time than is necessary to perform calibration (approx. 20 seconds). Thermal offsets produced by the relay coil may introduce an error in calibration when time in calibration is in excess of 20 seconds.

h. Initiate the zero calibration constant computation by entering this command:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

After entering the command, the display will update with the correct reading of the input.

i. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

j. Adjust calibrator output to 20 mA.

k. Wait at least 10 seconds to allow all FEM channels to be read.

1. Access the point used previously for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

m. Initiate the +full scale calibration constant computation by using this command:

[CLEAR] [PRGM] [CALIB] [40000]* [RUN]

* For low sensitivity configuration (configuration switch #1 CLOSED/ON), enter [4000] instead. After entering the command, the display will update with the correct reading.

n. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

o. Now list the calibrations constants for that FEM by entering this command:

[CLEAR] [LIST] [1] [CALIB] [fem no.] [RUN]

This command will give you a printout of the FEM's calibration constants. These constants will be most useful if you have to move this FEM to another slot or another Digitrend 245 data logger system, or if you decide to use this FEM in a remote application. Refer to 1.5.

CURRENT FEM CALIBRATION COMPLETED

1.4 HIGH VOLTAGE FEM CALIBRATION

Test Equipment Required:

Precision Voltage Source: resolution, 1 mV; accuracy $\pm$ .01%. Power Designs 2005A or equivalent.

1.4.1 Preliminary Set-up

a. Perform preliminary set-up per steps 1.2.1.a to 1.2.1.j.

b. Apply power to the data logger system, placing the keyswitch in PRGM. Allow 5 minutes warm-up time before proceeding to 1.4.2.

1.4.2 Calibration

a. Place the front panel keyswitch in PRGM if not already done.

b. Assign Function 6 to all points within the FEM:

[CLEAR] [PRGM] [POINT] [first point no.] [-] [last point no.]

[FUNC] [6] [RUN]

Specify the first and last points of the FEM according to its slot location. Refer to Table 1-1.

c. Adjust calibrator output to 00.000 volts.

d. Wait at least 10 seconds to allow all FEM channels to be read.

e. Log the points within the FEM:

[CLEAR] [LOG] [POINT] [first point no.] [-] [last point no.] [RUN]

f. Examine the log. If the voltage scatter of point values is less than 1 millivolt, calibration of the High Voltage FEM is not required. If the voltage scatter is greater than 1 millivolt, determine which point number has its value closest to the mid-point voltage scatter, then proceed to the next step.

g. Access the point number determined to be at mid-point for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

NOTE

Do not leave the High Voltage FEM in the calibration mode for more time than is necessary to perform calibration (approx. 20 seconds). Thermal offsets produced by the relay coil may introduce an error in calibration when time in calibration is in excess of 20 seconds.

h. Initiate the zero calibration constant computation by entering this command:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

After entering the command, the display will update with the correct reading of the input.

i. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

j. Adjust the calibrator output to 22.000 volts.

k. Wait at least 10 seconds to allow all FEM channels to be read.

l. Access the point used previously for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

m. Initiate the +full scale calibration constant computation by entering this command:

[CLEAR] [PRGM] [CALIB] [22000]* [RUN]

* For low sensitivity instruments (configuration switch #1 CLOSED/ON), enter [2200] instead.

After entering the command, the display will update with the correct reading.

n. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

o. Now list the calibrations constants for that FEM by entering this command:

[CLEAR] [LIST] [1] [CALIB] [fem no.] [RUN]

This command will give you a printout of the FEM's calibration constants. These constants will be most useful if you have to move this FEM to another slot or another Digitrend 245 data logger system, or if you decide to use this FEM in a remote application. Refer to 1.5.

HIGH VOLTAGE FEM CALIBRATION COMPLETED

1.5 USING THE STORED FEM CALIBRATION GAIN CONSTANTS

Your Digitrend 245 data logger system retains four calibration gain constants for every FEM. These gain constants are stored in battery backed RAM (random access memory). Your data logger refers to this information as data points are being linearized. (A particular point function will use one of these gain constants.) Due to the cumulative effect of component tolerances, a set of constants are unique for a particular FEM.

Whenever you finish calibrating a FEM, you should list its calibration gain constants and save the resulting printout. A good way to save this printout is to tape it on the FEM housing (though not on the removable cover, it may get swapped with another cover). Otherwise, without the gain constants on hand, you cannot just move a FEM from one location to another without affecting the overall accuracy of its readings. (Accuracy will be about $\pm$ 3.5% -- it will be necessary to perform the entire calibration procedure in order to bring the accuracy to specifications.) Also, should RAM memory be cleared (TP6 and TP7 shorted), you will have to perform the entire calibration procedure for all FEMs in the system unless you have the gain constants for those FEMs on hand.

The calibration gain constants are listed by using this command structure:

```
COMMAND STRUCTURE - List Calibration Gain Constants

  [CLEAR] [LIST] [device code(s)] [CALIB] [fem no(s)] [RUN]
```

FEM numbers (1-25) are specified in the command as any single number, any range of numbers, up to 4 separate numbers, or up to 4 separate groups of numbers. Refer to the discussion of the [-] and [ENTER] keys in 4.4.3.

The FEM number is determined by the FEM's slot location within a particular unit (mainframe or satellite #1-#4). Refer to Table 1-1 for the cross reference of FEM number and associated unit/slot location.

Here's an example list printout of the calibration constants:

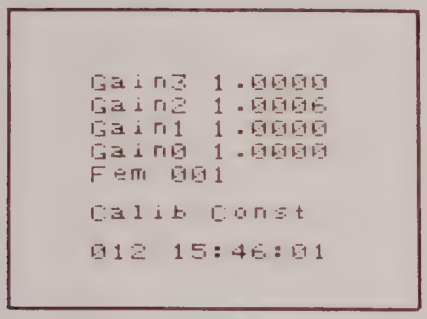


FIGURE 1-1. EXAMPLE LISTING OF CALIBRATION CONSTANTS

The typical situations for which you would use the saved calibration gain constants are:

(1) MOVING A FEM FROM ONE SLOT TO ANOTHER SLOT IN THE SYSTEM.

(2) INSTALLING A SPARE FEM FROM OFF THE SHELF INTO A SYSTEM.

(3) TRANSFERRING A FEM FROM ONE DIGITREND 245 SYSTEM TO ANOTHER.

(4) CALIBRATING A REMOTE FEM AT THE MAINFRAME, THEN REINSTALLING IT AT THE REMOTE LOCATION. (This makes calibration of remotely located FEMs easy and convenient.)

(5) WHENEVER THE BATTERY BACKED RAM MEMORY HAS BEEN CLEARED (TP6 AND TP7 SHORTED).

Use the following procedure to enter a FEMs calibration gain constants:

a. Short any convenient input (preferably one without a sensor attached).

b. Access the shorted input for calibration by entering this command:

[CLEAR] [CALIB] [POINT] [point no. of shorted input] [RUN]

c. Initiate the zero calibration constant computation by entering this command:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

d. Exit the calibration mode by entering this command:

[CLEAR] [RESET] [CALIB] [RUN]

e. Enter the gain constants (referring to the list that you saved) for the FEM by using this command structure:

COMMAND STRUCTURE - Program Gain Constants

[CLEAR] [PRGM] [constant] [FUNC] [fem no.] [-] [gain no.] [RUN]

NOTE 1: This command must be entered with a program enabled device.
NOTE 2: For some calibration constants, you may find a .0001 difference between the entered number and the listed number. This is normal and is due to the 16-bit math internal to the microprocessor. The effect on accuracy is insignificant.

You will have to enter this command four times to enter all of the gain constants of a particular FEM.

The specified constant will always be a five-digit number, for example, 1.0045. The decimal point in the constant is entered as a hyphen [-]. Thus, a calibration constant of 1.0045 is specified in the command as [1] [-] [0045].

A calibration constant is directed to a particular FEM slot by the [fem no.] entry. This entry is a single number from 1 to 25. Make sure that you specify the right FEM no. for the calibration constants you are entering and the intended location of the FEM. Refer to Table 1-1 for the cross reference of FEM number and associated unit#/slot location.

The gain no. entry is a single number from 0 to 3. This entry specifies a particular gain constant to be programmed. If you look at the example printout above, you will see that the four constants are labeled Gain0 through Gain3 (which in this example are for FEM #1).

Repeat steps 1.5.a through 1.5.e for each additional FEM that requires gain constants to be entered.

2 Theory of Operation

2.1 INTRODUCTION TO THE THEORY OF OPERATION

In this section, we will provide a technical discussion on how the Digitrend 245 data logger system operates. This discussion is geared to readers with a technical background in electronics. The information presented should help in understanding the system when troubleshooting.

2.2 MAINFRAME BOARDS, GENERAL

The mainframe boards control and support the basic functions required by the data logger. The following printed circuit board assemblies comprise the mainframe boards:

1. Central Processor Unit (CPU) board
2. Interface board
3. Peripheral Interface Adaptor (PIA) board
4. Front Panel board
5. Power Supply Module

The CPU board is the functional brain of the Digitrend 245 data logger system. This board contains, among other things, a 16-bit microprocessor and system memory--both of which are vital for operation of the data logger system.

With the use of opto-couplers, the Interface board (mounted on the inside of the mainframe's rear panel) interfaces all serial communications to the CPU board. All satellite units, external serial I/O devices, and remote start inputs are physically connected to the Interface board.

The PIA board interfaces the FEMs and front panel readout functions (i.e. display and printer) to the CPU board.

The Front Panel board provides the man/machine interface. The seven segment LED, status LED indicators, and audible beeper are driven by this board. Additional functions are performed by the keyboard decoding circuitry and the thermal printer control/driver circuitry.

Regulated power to all circuits is provided by the power supply module. The power supply design incorporates overvoltage and short circuit protection. Both mainframe and satellite use the same type power supply module.

2.2.1 CPU Board Assembly, General

Assembly: 245-4110-xx
Schematic: 245-6110-xx

The Digitrend 245 mainframe unit can be viewed as any other computer system that consists of a central processor unit (CPU), memory, and input/output (I/O) interfaces. The CPU board itself comprises a large part of the system.

Operation of the data logger revolves around the 16-bit 68008 microprocessor on the CPU board (4E). This microprocessor uses an 8-bit data bus which is totally separate from the address lines (non-multiplexed). This scheme combines the advantages of 8-bit (low cost) and 16-bit (high performance) systems. Both address and data busses are buffered to external devices. This provides a measure of input protection to the CPU and minimizes the effects of bus loading.

The CPU board also contains a crystal controlled master clock, real time clock, system memory with battery backed RAM, and six serial I/O ports. The CPU board interfaces to the rest of the system through the system bus, executing the program which forms the basis for all decision making processes, providing system timing and control signals, and monitoring system operation.

2.2.1.1 Address Bus

The address bus is outgoing from the CPU. (An interrupt is vectored through the data bus.) Various control signals are derived from the address lines through the use of decoders.

A major block address decode function is performed by ROM 4D. From ROM 4D, the AD BUS is formed which is given as input to ROM 2E and buffer 3D. Major block decode of the memory map is provided at the output of buffer 3D.

Decoders 3C and 3L provide address decoding to individual devices on the control bus.

Address lines to devices outside the CPU board are buffered by buffers 3A and 3B.

2.2.1.2 Data Bus

The 8-bit data bus is a tri-state bidirectional bus. The data bus handles the interrupt vector when IACK(not) (from decoder 4F pin 7) is low. Data outgoing from the CPU is buffered by buffer 2A. Data incoming to the CPU is buffered by buffer 2B.

2.2.1.3 CPU Clock Generator

The CPU is driven by a single phase clock consisting of crystal oscillator 5F and synchronous 4-bit counter 5G.

Crystal oscillator 5F provides the clock input (15.72864 MHz) for counter 5G, pin 2. The counter provides two outputs. The input frequency is divided by two at 5G pin 14 (7.86432 MHz) to provide the F8 signal on the control bus. F8 is used to provide the CLK input to the microprocessor. The input frequency is divided by sixteen at 5G pin 11 to provide the E signal on the control bus. This signal synchronizes the various peripherals which communicate to the microprocessor. Resistors R40 and R41 minimize overshoot and undershoot of the counter output.

2.2.1.4 Real Time Clock

The real time clock keeps track of time when power is off. This circuit is on page 5 of the schematic. The real time clock consists of decoder 5L; counters 5P, 5N, and 5M; latches 4L, 4M, and 4N; and crystal Y1 and associated components. All of the ICs in this circuit are powered by the Vbb bus. When power goes down, the reset signal applied to counters 5N and 5M is removed. These counters then count the seconds which comes from the crystal controlled counter at 5P pin 3. When power comes back up, the real time clock's accumulated seconds are read into the CPU by sequentially dumping the latches onto the data bus. This is done by decoder 5L which is enabled by the R/W(not), DS(not), and RTC(not) signals. Address lines A0-A3 determine the latch to be read on the data bus.

2.2.1.5 DTACK Multiplexer

An active low handshaking signal called DTACK (Data Transfer Acknowledge) signals the MPU that a data transfer is complete. The DTACK(not) signal can result from a variety of sources. These sources include data transfers of ROM, RAM, off board peripherals, DUARTs, and the real time clock. It is the function of the DTACK multiplexer to route the proper DTACK source to the MPU DTACK(not) input at 4E pin 31. The DTACK multiplexer circuit (on page 3 of schematic) consists of shift register 5B, mux 4B, and transistor Q13.

The DS(not) signal is the conditional signal that enables mux 4B. Address lines A15-A17 then select the DTACK input that will be passed on to the MPU via the Z output of 4B pin 5. The Z output turns on Q13 which grounds the +5V pull-up at the MPU DTACK(not) input.

ROM and RAM data transfers are indicated by the VPA(not) and OFFBD(not) signals. Because of timing considerations, these signals are clocked through 5B by the F8 signal.

2.2.1.6 Interrupt Request (IRQ) Priority Encoding Circuit

The Interrupt Request (IRQ) Priority Encoding circuit consists of decoder 4G, NANDs 4H and 4J, flip-flop 5K, priority encoder 3K, and buffer 2K. (See page 3 of schematic.) This circuit gives the MPU the interrupt from the various MPU peripheral devices according to the hardware assigned priority. The priority of the IRQ signals, from highest to lowest, is as follows:

Interrupt	Level
DSP IRQ	6
SYS IRQ(not)	5
SPARE IRQ 1(not)	4
DUART 1 IRQ(not)	3
DUART 2 IRQ(not)	2
DUART 3 IRQ(not)	1

The priority encoder (3K) detects the highest order line (one through six) that is at a low level. The resulting outputs from 3K (pins 4, 6, and 15) are gated (by 4J) with the latched NMI(not) signal to provide a particular input to the MPUs Interrupt Control pins (4E pins 41 and 42).

With a level 2 interrupt (DUARTs) asserted on the Interrupt Control pins, the state of the DUART IRQ(not) pins is presented to the data bus by buffer 2K which is enabled by the LEVEL 2 IACK(not) signal. The LEVEL 2 IACK(not) signal originates from decoder 4G pin 13. The decoder outputs are derived from the IACK(not) signal in conjunction with address lines A1-A3. This decoder also produces the VPA(not) signal which signals the MPU that the device or region addressed is a valid peripheral address. The VPA(not) signal is also used to indicate that the MPU should use automatic vectoring for an interrupt--such is case with a level 2 interrupt in the data logger system.

2.2.1.7 ROM

ROM consists of four 32K x 8 EPROMs (2E, 2F, 2G, and 2H). Basic ROM decoding originates from one half of decoder 3C (on page 3 of schematic). A particular EPROM is selected by a combination of address line inputs A15 and A16 in conjunction with the ROM(not) signal from buffer 3D (on page 2 of schematic).

2.2.1.8 RAM

The RAM area is composed of CMOS, battery backed-up RAM chips 1E, 1F, 1G, and 1H (each 8K x 8). Basic RAM decoding originates from the other half of decoder 3C (on page 1 of schematic).

A particular RAM is selected by a combination of address line inputs A13 and A14 in conjunction with the RAM(not) signal from buffer 3D (on page 2 of schematic).

To maintain RAM data integrity, read/write of RAM is tightly controlled by gating the WPRO, WREN(not), R/W and DS(not) signals. (See page 1 of schematic.) This produces the RAM read/write signals R/W(not) and WE(not).

A write attempt to RAM with a wrong combination of control signals will result in a WRERR(not) signal. This signal is sent to the CPU for arbitration.

To ensure data integrity, transistor Q5 inhibits RAM selection (chip enables at Vbb) when system voltage falls low, or upon resets.

2.2.1.8.1 RAM Battery Back-up System

CPU RAM memory is provided with battery back-up circuitry comprised of Q6, Q7, BT1, R14, R15, and C5. (See page 1 of schematic.) In normal operation, Q6 is forward biased by +5 V at the emitter, which supplies a trickle charge to BT1 via resistor R14, and providing Vbb for RAM memory from the collector. Vbb tracks the +5 volt bus until the voltage drops below 3.6 volts; thereafter, Vbb is held at +3.6 volts via transistor Q7 and battery BT1. Since Q6 is turned off by the battery voltage with the emitter below +3.6 volts, battery back-up is confined to the Vbb bus. C5 decouples any transient noise to ground. RAM memory is cleared by shorting testpoints TP6 and TP7 together which grounds Vbb.

2.2.1.9 +5 Volts Low Detect Circuit

The +5 Volts Low Detect circuit (see page 5 of schematic) uses an LM393 op amp (3N) to compare the +5 volt bus, via R18, to a reference voltage across CR1. Potentiometer R18 is used to adjust the division ratio of the 5 volt line. When the 5 volt line drops below about 4.75 volts, the first op-amp output swings negative, causing the second op-amp to also swing negative which in turn triggers the reset circuit. (This is one of two reset inputs to the halt/reset circuit.) R16 and C20 act as a filter for the 5 volt line, and R20 increases the hysteresis of the detector. C22 and C23 provide line filtering.

2.2.1.10 Halt/Reset Circuit

The halt/reset circuit consists of diodes CR2-CR5; transistors Q8, Q9, and Q10; and associated components. (See page 5 of schematic.) This circuit is basically a switching circuit that drives the RESET(not) line low when a reset of the CPU is required. Darlington Q8 and zener diode CR4 establishes a threshold level of about 4.75 volts below which Q9 will turn on and provide a low level to the RESET(not) line. To ensure proper operation of the CPU circuits when power is reapplied, capacitor C26 introduces a delay in the removal of the RESET(not) signal until the CPU is fully powered (greater than 4.75 V).

There are two inputs to the halt reset circuit that can cause a reset. One input is the low +5 volt detect circuit which was discussed above. The other input is the RREQ line. This is the

software request for a reset. When RREQ is high, Q10 is turned on and drives the input to the halt/reset circuit low. This in turn drives the RESET(not) line low which resets the CPU.

There are two inputs to the halt reset circuit that can inhibit the RREQ. These are the WATCHDOG DISABLE(not) input and a closed switch S1. With WATCHDOG DISABLE(not) low, Q10 will never turn on, overriding the RREQ input. The same effect is achieved with switch S1 closed. However, a low +5V buss condition can still trigger a reset.

2.2.1.11 Serial Communications

Serial communications to the CPU is supported by DUARTS 1L, 1M, and 1N. (See page 4 of schematic.) DUART stands for Dual Universal Asynchronous Receiver/Transmitter. This particular device provides two independent full-duplex asynchronous receiver/transmitter channels in a single package.

A particular DUART is selected by decoder 3L (on page 3 of schematic) from pins 9, 10, and 11.

The operating mode and data format of each channel is programmed independently through software instruction. The baud rate is also software selectable and is derived from crystal oscillator 1K. The data logger operating system program fixes the baud rate for satellite communications at 4800 baud. The baud rate for the two external serial peripheral devices is selectable by a data logger programming command which addresses the DUART channel accordingly.

DUART 1L provides serial communication for the two external serial peripheral devices. DUART 1M provides serial communication for satellites #1 and #2. Four auxiliary input ports of DUART 1M receive the four remote start inputs. DUART 1N provides serial communication for satellites #3 and #4.

2.2.2 Interface Board, General

Assembly: 245-4100-xx
Schematic: 245-6100-xx

The Interface board interfaces various serial devices to the mainframe CPU. These devices include the four satellite units and the two serial peripheral devices. The Interface board also couples the remote start inputs to the CPU via opto-couplers.

2.2.2.1 Satellite Communications

Each satellite communicates over a 20 mA current loop for which the Interface board provides a passive transmitter and receiver. (See page 2 of schematic.) This discussion will center on satellite #1 circuitry since the same circuit is used for satellites #2-#4.

The transmitted data from the CPU board DUART (TX2A) to satellite #1 is buffered by Z8 pins 6 and 14 which drives opto OC6. When TX2A is high (MARK), the output transistor of OC6 is turned off, allowing Q5 to flow the full loop current. When TX2A is low (SPACE), the output transistor of OC6 is turned on, limiting the loop current through Q5 to less than 2 mA.

The received data from satellite #1 to the CPU board DUART is opto-coupled by opto OC5. A MARK will turn on the output transistor of OC5 which causes a logic high across R33. A SPACE will turn off the output transistor of OC5 which causes a logic low across R33. This signal is buffered by Z8 pins 11 and 9 to drive the RD2A line to the CPU board DUART.

2.2.2.2 Serial Peripheral Device Communications

Handshaking and data signals for serial peripheral devices come from the CPU board DUART. The Interface board provides separate circuits to each peripheral device to condition these signals for RS-232 or 20 mA current loop communication. (See page 1 of schematic.)

Signals sent to RS-232 type devices (RTS and Transmitted Data [TX]) are buffered by RS-232 drivers (Z6 and Z7). Signals received by RS-232 devices (DCD, CTS, and Received Data [RD]) are buffered by RS-232 receivers (Z3 and Z5). The output from the RS-

232 receivers are inverted and buffered by NAND gates (Z1) for input to the DUART.

The transmitted and received data are also opto-coupled to a 20 mA current loop using a series pass transistor with zener controlled base drive to limit loop current. Switch assemblies S1 and S2 are used to select internal (active) or external (passive) power for the transmit and receive loops.

For transmitted data, a MARK or SPACE will turn on or off respectively the output transistor of the transmit loop opto (OC2 and OC4) and the series pass transistor (Q2 and Q4). This in turn causes full current (20 mA) or limited current (less than 2 mA) to flow in the transmit loop.

The receive loop works in a similar fashion to the transmit loop. A MARK or SPACE (current on or off) will turn on or off respectively the output transistor of the receive loop opto (OC1 and OC3). This in turn causes a low or high level on the collector. The signal at the collector is inverted and buffered by NAND Z1 to the RD line to the DUART.

2.2.2.3 Remote Start Inputs

The four remote start inputs are isolated from the CPU board DUART by opto-couplers OC11 and OC12. (See page 2 of schematic.) A remote start of a log is initiated with a contact closure at the appropriate pair of J5 terminals. This action shunts the +5 V drive to an opto LED causing it to turn off. This in turn causes the associated opto transistor to turn off and a high level signal to appear on its collector. The collector signal is buffered by Z9 and sent to the DUART remote start inputs where it is then read by the CPU.

2.2.3 PIA Board, General

Assembly: 231-4310-xx
Schematic: 231-6310-xx

The PIA board interfaces the Front Panel board and FEM assemblies to the CPU. The PIA board uses three 6821 peripheral interface adapters for these tasks, two for the Front panel interface, and one for the FEM interface.

These adaptors allow interfacing of the external signals generated by the Front Panel board and FEM to the CPU as well as interfacing CPU signals to the external circuitry (Front Panel board and FEM).

The PIA board can be divided into seven functional sections:

1. FEM INTERFACE
2. BINARY COUNTERS
3. FEM INTERFACE CIRCUIT AND SERIAL ENCODER
4. WATCHDOG CIRCUIT
5. WRITE PROTECT HANDSHAKE CIRCUIT
6. DISPLAY PIA AND PRINTER PIA
7. DATA BUFFER ENABLE/DATA, ADDRESS, AND CONTROL BUFFERS

2.2.3.1 FEM Interface

PIA 4B provides the interface between the CPU and FEMs. (See page 1 of schematic.) Data from the CPU to the FEM consists of a 16-bit data stream which starts the FEM and PIA counters, initializes the FEM A/D converter, and provides configuration data to accommodate the data point being measured. Data from the FEM to the CPU consists of the latched count value from the PIA binary counters initiated by the zero cross detect pulse from the FEM, or detection of an over-range condition (input overload or broken thermocouple). FEM data is input/output on 4B pins 2-9 (peripheral data register A) and forms the basis for DATA BUS 2.

2.2.3.2 Binary Counters

The counter circuitry consists of two sequential binary counters, a high order counter and a low order counter (4F and 4C respectively). These counters, which are continuously driven by the CPU clock (BF1), provides the raw counts which represents the FEM data point value when a zero cross is detected. The counters also provide the various signals (f6, f7, and f17) which modulate the FEM serial data from shift registers 5C and 5D for serial transmission to the FEM. The higher stages of the counter (lower frequencies) are reset from the system reset line (BRESET) to provide a minimum time from reset to the first post reset NMI. The lower stages of the counter are reset from a power supply sync circuit that synchronizes phase1 and phase2 from the power supply square wave output, with the CPU NMI. The power supply timing interface (phase1 and phase2) is required for proper operation of the FEMs, as FEM timing is derived from this source.

2.2.3.3 FEM Transmit and Receive Interface

The CPU to FEM data is output from peripheral data register A (4B, pins 2-9). This data is sequentially output in two 8-bit bytes to shift registers 5C and 5D. The same data register is used to read the latched counter value from latches 4D and 4E when a zero cross, or an overload condition is detected. The output from these latches are read sequentially in two 8-bit bytes.

The gamma0 and gamma1 lines (4B, pins 16 and 17) are used to select which of the four registers (4D, 4E, 5C, and 5D) are to be active on DATA BUS 2.

CPU to FEM data is output as follows:

Gamma0 and gamma1 (4B pins 16 and 17 respectively) are NANDed (3Ca, 3Cd) with E0 (4B pin 19) to select the operating mode of shift registers 5C and 5D. When pin 9 of the shift register is high, the data on DATA BUS 2 is parallel loaded onto the shift register. When pin 9 of the shift register is low, data within the register is shifted synchronously with the positive transition of the clock. Shift register 5C is loaded with the FEM programming data. Shift register 5D is loaded with all "ones". When the correct data appears on the shift register inputs, the data is loaded in by a high on pin 9 of that register. When both registers are loaded, pin 9 of both registers goes low and the data is ready to be shifted for encoding.

The 15 Hz clock (f17) initiates the shifting/encoding sequence. When the 15 Hz clock is low, a high appears on the clock input of flip-flop 5Fb, clocking the state of the CLEAR input (which is high) onto the Q output. In addition, the high transition to the clock input is coupled by capacitor C1 to the CLEAR input of flip-flop 1Ab pin 10. This forces the Q output at 1Ab pin 13 low if no zero cross was detected. This causes latches 4E and 4D to latch the zero count from counters 4F and 4C (the instant f17 goes low, the counter stages revert to zero). The latched zero count is read into the PIA (E1 high) via DATA BUS 2 and interpreted as an over-range or broken thermocouple condition. Thus, the latch, read, and reset sequence is completed whether or not a zero cross pulse was received to initiate the sequence.

Flip-flop 5Fb is controlled by counter 1B and is used to enable NAND 3Fb utilized as a pulse gate. The pulse gate is enabled for the duration of 16 clock pulses (modulated data). Counter 1B counts the DATA 0 pulses. When 16 pulses are counted, 1B pin 5

(E2) outputs a high which resets 5Fb via exclusive-OR 5Ea used as an inverter. This forces the output at 3Fb to remain high until E0 goes high (1B reset) and f17 goes low, whereupon another cycle of data shifting/encoding is begun.

The data shift/encode circuitry is comprised of flip-flop 5Fb, exclusive-OR 5Ea and 5Eb, inverter 1Ec, and counter 1B. The timing diagram in Figure 2-1 shows the signal relationships in the data encoding scheme. Refer to this timing diagram when reading the following paragraph which explains how the data shift/encode circuit operates.

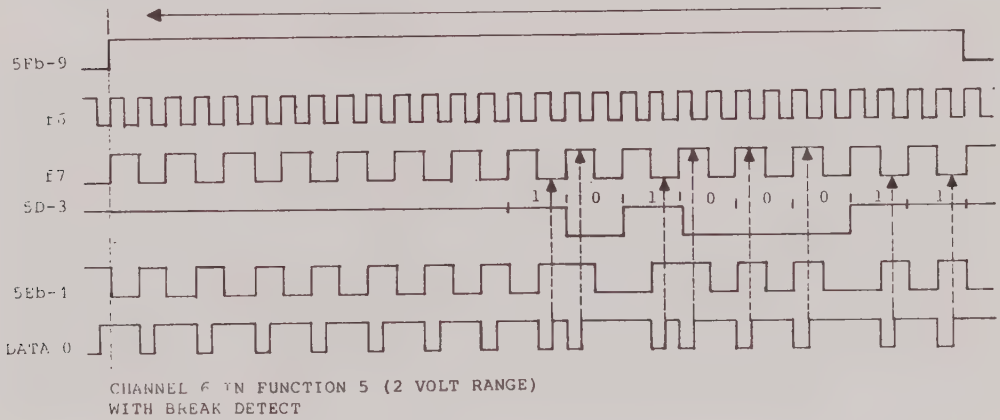


FIGURE 2-1. DATA ENCODING FOR FEM SERIAL TRANSMISSION

Data shifting/encoding is done as follows:

The data is input to 5Eb where it is exclusive-ORed with 15 kHz (f7). This results in the 15 kHz signal being modulated by the data. When the data appearing at 5Eb pin 5, is high, the output of 5Eb is 15 kHz out of phase with f7; when the data is low, the output is 15 kHz in phase with f7. The 15 kHz output from 5Eb is NANDed with 30 kHz (f6) which results in a 15 kHz output delayed by 1/2 cycle from the 15 kHz input and with 25% more duty time than the 15 kHz input. The net result is that the positive transitions of the modulated data occur mid-point of the 15 kHz state (f7) opposite the data. If the data is high, positive transitions of the modulated data (DATA 0) occur exactly mid-point of f7's low cycle. If the data is low, positive transitions of DATA 0 occur

exactly mid-point of f7's high cycle. Whether the data is "one" or "zero" results in a positive transition from DATA 0 which serves to shift out the next bit from 5D pin 3. The FEM detects the logic level by comparing the positive transitions with the 15 kHz clock. When the positive transitions occur in relation to the clock determines the logic state.

Two multiplexed loops are used by the PIA card to serially transmit and receive FEM data. (A simplified schematic of this circuit function is shown in Figure 2-9.)

DATA 0 is transmitted to the FEM by controlling a current loop consisting of multiplexer 2B, de-multiplexer 3B, and the FEM receive opto-coupler. Multiplexer 2B supplies the current source; de-multiplexer 3B supplies the current sink. DATA 0 turns on/off the current source/sink depending on the transitions made by DATA 0. The beta lines (beta0-beta2) are used to vector the FEM to which data is being transmit.

The FEM zero cross pulse is received by the PIA card on a loop consisting of multiplexers 2A, 3A, and the FEM transmit opto-coupler. Multiplexer 2A supplies the ground return for the FEM's opto-coupler transistor. Multiplexer 3A supplies the +5 volts pull-up for the FEM's opto-coupler open collector. The alpha lines are used to vector the FEM from which the zero cross pulse is to be received.

The transmit/receive loops operate simultaneously; both addressing a different FEM sequentially in an interlaced manner. As one FEM is addressed for programming, another is being addressed for the zero cross pulse.

When the FEM detects a zero cross, a pulse is generated by the FEM which sinks the +5 volt pull-up (3A) to ground (2A) via the FEM's transmit opto-coupler. The resultant low appears on the D input of flip-flop 1Ab, and clocked in by f1 (1 MHz), latching the Q output of 1Ab low via feedback resistor R7. The Q(not) output is inverted by 1Eb, providing E3 which serves to latch the count value of 4F and 4C onto latches 4D and 4E. At the same time the Q output of 1Ab latches low, the Q(not) output goes high; inhibiting receive multiplexers 2A and 3A.

With the count value latched in, the two latches are then sequentially output onto DATA BUS 2 by inputing a low on the OE input one at a time. NANDs 3Cc and 3Cb control the OE inputs. E1 is an enable for OE, and gamma0 and gamma1 selects one of the two

latches. After the contents of both latches are output on DATA BUS 2, the CPU receives this data from PIA 4B and converts the counts into a discrete point value.

2.2.3.4 Watchdog Circuit

The watchdog circuit is comprised of flip-flops 1Fa, 1Fb, and 2Eb; NANDs 3Ec, 3Ed, and 3F; NOR 2Fb; inverter 3Dd; and counter 2Db. This circuit alternately monitors the data being transmitted to the FEMs (CATCH1[not]), and the scan clock being transmitted to the front panel displays (CATCH2[not]) for any dropout in the signals. If a dropout occurs, a reset request (R REQ) is sent to the CPU.

The watchdog circuit also accepts the RES REQ line from PIA 2H, pin 17, via inverter 3Dd. This line allows the microprocessor to reset the system on power down, or if a failure is detected.

The R REQ signal, generated by the watchdog circuit, is sent to the CPU board to provide a system reset. The system reset (BRESET[not]) then clears the watchdog circuit.

2.2.3.5 Write Protect Handshake Circuit *

The write protect handshake circuit is comprised of flip-flops 1Ca, 1Cb, 1Da, 2Da, 2Ea, and 1Db; NORs 2Fa and 2Fc; inverters 1Ee and 1Ef; and NANDs 3Eb and 3Fc.

When the CPU detects a write protected memory location, it transmits a WRPTA signal to the system. If the CPU has opened the WPR window by toggling the PRO REQ line high, the WPRO(not) line will be high, indicating a write to this location is legal.

If the WPRO(not) line is low when the CPU attempts to write to a WPR location, VMA is retracted, and R/W is taken to the read state (high), and the system is reset by the CPU board, indicating a write failure has occurred.

When the CPU opens the WPRO(not) line, two types of counters are used to ensure the window does not malfunction. One counter consists of flip-flops 1Ca and 1Cb. These flip-flops advance the PRO REQ line to the reset of the WPRO(not) line, allowing WPRO(not) to be enabled for 500-700 microseconds only.

* NOTE: This is an inactive circuit in the Digitrend 245 data logger system. This circuit is active only for the Digitrend 235 data logger which also uses the PIA board.

The second counter, consisting of flip-flops 1Da and 2Da, counts the number of writes to WPR memory, which serves to close the window after the third write. Therefore, the CPU may either write a byte of data, or an address (2 bytes) into memory with the WPRO window open. No more than three consecutive BF1 periods of write to protected memory are permitted. Thereafter, the window is closed, and must be reopened for further writes.

NAND 3Eb and flip-flop 2Ea inhibits the NMI line during WPRO(not) legal writes, to prevent NMIs from extending the WPR window beyond the defined time allocated to it.

Write protected RAM is used to store calibration data, alarm setpoints, back-up copies of the job tables, and system configuration data.

2.2.3.6 Display PIA and Printer PIA

In addition to the FEM PIA, two additional PIAs are used in the PIA card. One PIA (2H) controls the operation of the front panel keyboard/display/ buzzer circuits. The other PIA (3H) controls the thermal printer circuits.

PIA 2H interfaces the CPU to the display LEDs, the keyboard decode matrix, the buzzer, and the write protect and reset request circuits. For display, the PAx lines are programmed as outputs; each output controlling one segment of the LED display, and input to the appropriate transistor driver on the Front Panel board. Scan clock toggles whenever the PAx lines are read, and scan reset is level programmed through the B side control register.

For the keyboard, the PB0-PB3 lines are programmed as inputs. PB4 is an input line for the keyswitch PRGM(not) signal, and PB5-PB7 are output lines for BUZZ(not), PROREQ, and RESREQ. The buffered low line, BLOWL, is an edge triggered input to the PIA, which is used to signal the CPU that the power supply primary voltage is dropping low. The source for this signal originates from the power supply card.

For the printer, all port lines in PIA 3H are programmed as outputs. These outputs are routed to the printer via the Front Panel board drivers 2E, 3E, and 4E (refer to Front Panel board schematic 231-6320-xx). The control lines are level outputs (CA2 and CB2), and edge triggered inputs (CA1 and CB1).

2.2.3.7 Address/Control and Data Buffers

All data and address lines on the PIA board are buffered by LS245 buffers, 4A and 5A, before entering the board.

Address buffer 5A (for addresses, F1, and PER1[not]) is always enabled to transmit into the PIA control bus 1.

Data buffer 4A is bi-directional, and is controlled by the buffered R/(not)W line and the enable data buffer (EDB[not]) line. The data buffer enable circuitry provides the EDB(not) line and is comprised of NANDs 1Ha and 3Ea; NOR 2Fd; and inverters 1Ed and 2Cd. All inputs to 1Ha must be high to enable data buffer 4A; as a result, the data buffer is enabled only during a high cycle of BF1. The R/(not)W line controls the direction of the data buffer, and is inverted by 2Cb to provide the DIR input for 4A. Inverter 2Cc inverts the inverted R/(not)W to provide BR/(not)W for use elsewhere on CONTROL BUS 1.

2.2.4 Front Panel Board, General

Assembly: 231-4320-xx
Schematic: 231-6320-xx

The Front Panel board provides the man/machine interface with the data logger system. It contains the drivers for the LED display, encoding circuitry for the keyboard, drive circuitry for the audible beep, and control and drive circuitry for the printer head and motor. All Front Panel board circuits are under software control through the PIA board interface to the CPU.

The Front Panel board can be divided into four functional sections:

1. DISPLAY DRIVE CIRCUITS
2. PRINTER CONTROL CIRCUITS
3. RESET INTEGRATOR
4. BUZZER CIRCUIT

2.2.4.1 Display Drive Circuits

The display circuitry is arranged in a display matrix, using common segment lines (SEG A through SEG H), driven from PIA port A on the PIA board. A low on any of the common lines will enable a constant-current source, supplying 180 mA per segment. The segments are illuminated when the common cathode of the display is low; completing a path of conduction for the LEDs within that display.

The cathode of each display and LED (DS1-DS17) is connected to the output of two Darlingtons connected in parallel, using Darlington transistor arrays 1C and 1B. The parallel configuration provides higher load current capability. The Darlingtons sink the appropriate cathode when the input, controlled by Johnson counter 2C, is high. The buffered outputs of the Johnson counter (E0-E9) multiplexes the display and LED indicators by sinking the cathodes sequentially one at a time at the rate of the SCAN CLOCK(not) input. The buffered outputs are also used for the decode scan of the keyboard and configuration diodes.

Configuration diodes are installed in spare slots in the keyboard matrix. These diodes are switched "in" or "out" by DIP switches S1-S3. As the matrix is scanned, a diode with an "on" switch will pull the associated line (E7-E9) high. These lines are buffered (2A), then returned to PIA 2H (on the PIA board) port B low order bits (KYBD0-KYBD3).

With each scan cycle, the display and keyboard inputs are strobed, and the configuration diodes are read and stored for interpretation.

The scan is reset by the SCAN RES line, and clocked by the SCAN CLOCK(not) line; both originating from PIA 2H on the PIA board.

2.2.4.2 Printer Control Circuits

The thermal printer prints a line of 12 characters (max) wide in a 5 x 7 dot matrix. Each line is printed sub-column by sub-column (1-5) and sub-row by sub-row (1-7) on all 12 characters simultaneously until the entire line is printed.

Two one-shot timers on the Front Panel board are used to control the thermal printer.

One-shot 4Ab controls the burn-time of each sub-column. Transistors Q1, Q2, and associated circuitry are used to vary the charging rate of C2, which varies the pulse width of the Q(not) output, and hence, the burn-time. After receipt of the BURN START positive transition, 4Ab times out and BURN STOP is output, and a new sub-column is ready to be burned (printed). Johnson counter 4C sequentially burns each sub-column with the receipt of a BURN START input on the clock. The burn pattern for a particular character is determined by the COL1-COL12 lines originating from the printer PIA, and is taken from the resident program by the CPU.

One-shot 4Aa advances the printer motor one sub-row after a period of time determined by R1 and C1 has elapsed. The elapsed time is from the negative transition of DOT STEP, and provides sufficient time for the printer to print one entire sub-row 12 characters across before the next sub-row is to be printed. As the the motor is stepped to the next sub-row by DOT CLOCK, counter 4C is cleared, and each sub-column of the new sub-row is then sequentially burned. After all five sub-columns are burned, the process repeats itself until all seven sub-rows have been processed, which completes the printed line. Thereafter, the motor steps a line space by several DOT STEP/DOT STOP cycles and a new line of information is begun.

2.2.4.2 Reset Integrator

System resets are of two types; power "on" reset, and system failure reset. The latter may originate from either a hardware failure, or a software error. The reset integrator (3B) counts failure resets, and stores this information for approximately 48 hours after the last failure reset.

On power up, all integrator flip-flops in 3B are cleared. Any reset after power up will cause a falling edge on the reset line, which will clock through the flip-flops via NOR 4Bd. The "zero" on the input of the shift register formed by these flip-flops will clock through to the successive stages with each reset pulse.

The first and third stages are connected to remove configuration diodes 11 and 12 on the respective post power up reset. The CPU monitors these diodes, and will output a "RESET" message after the

first such reset. After the third reset, with both diodes now removed, the CPU will reset jobs (call original program information from protected RAM), and output a "RESET JOBS" message.

As the first RESET is detected, the TIME E(not) line goes low, and counters 3D and 3C start to count the number of display scans. When both counters overflow, reset integrator 3B will be automatically reset by OVEC. The counter period is approximately 48 hours. If no resets occur to reset the counter during any 48 hour period following the previous reset, the counter overflow will clear the reset integrator, clearing the system record of post power up resets.

2.2.4.4 Buzzer (Beeper) Circuit

The buzzer circuit consists of a pair of one-shots (1E), transistor drivers (Q21, Q22), and a piezo-electric transducer (Y1). One-shot 1Ea is wired as a timer, to determine the duration of the buzzer. This one-shot is triggered by the falling edge of the BUZZ(not) line from the display PIA on the PIA board.

One-shot 1Eb is triggered initially by the output of 1Ea. It then re-triggers itself until 1Eb times out. This action creates a square-wave oscillation frequency of approximately 3 kHz. The Q and Q(not) outputs of 1Eb serve as base drives to drivers Q21 and Q22, which in turn energizes transducer Y1 which produces the beep sound.

2.2.5 Power Supply Module, General

Assembly: 231-4500-xx
Schematic: 231-6500-xx

The power supply board is used in both mainframe and satellite units to produce DC power for various circuitry. The line voltage is filtered for RFI rejection, rectified to give about 300 Vdc, and then reduced to about 116 Vdc by a switching regulator.

A power inverter, driven by a phase-locked oscillator, supplies two square-wave outputs that are rectified and filtered to give +5, +16, and -16 Vdc. Two regulated voltages of +12 and -12 Vdc are obtained from the +16 and -16 Vdc supplies, respectively.

The Power Supply can be divided into five functional sections:

1. INPUT CIRCUITS
2. SWITCHING REGULATOR
3. REGULATOR/CONTROLLER
4. OSCILLATOR, DRIVER, AND INVERTER
5. OUTPUT REGULATORS AND FILTERS

Each of these sections is described in the following paragraphs.

2.2.5.1 Input Circuits

A Pi filter is used in the high and low power leads to exclude RFI from the power supply input, and to prevent switching spikes from getting into the power leads.

A keyswitch is used to turn the instrument on or off, or to put it in the program mode. In the latter case, a ground is placed on the PROGRAM line to P1 pin A, to output a low to the PIA PROG line.

The ac input is full-wave rectified by CR31 through CR34, then filtered by C26 and C27. Jumpers are inserted at the fuse block (as shown on the schematic) for 115 VAC operation, to form a voltage doubler network that supplies approximately 300-350 Vdc to the switching regulator.

For 230 VAC line operation, no jumpers are required. The 230 VAC

line is full-wave rectified to again provide approximately 300-350 Vdc to the regulator.

Spark gaps SG1 and SG2 will arc over (and thereby blow the fuse) if more than about 470 volts is sent to the switching regulator. This prevents excessive line voltage from destroying the switching regulator.

2.2.5.2 Switching Regulator

The switching regulator reduces the unregulated 300 Vdc to a nominal 116 Vdc. The switcher is a free-running power oscillator that charges T3, a 3mh ferrite core inductor, then dumps the stored inductive energy into C7.

When Q16 turns on, the collector current ramps upwards until it reaches about 1.0 amp. At this point Q15 is turned on, which removes Q16's base drive (supplied by Q14). Q16 then shuts off, and CR45, R50 and C29 form a snubber circuit that absorbs some of Q16's switching energy and further turns on Q15 by increasing its base drive through R51. The collector-emitter voltage of Q16 rises until it is stopped by the "catch diode", CR44.

At this point, the inductor's voltage has gone from about +220 V to -116 V, and the inductor's current begins to ramp down towards zero. The average current through the inductor is about .5 A; thus, the maximum power transfer from the switching regulator is .5 A x 116 V = 58 watts. In practice it is actually less than this because there is a small amount of dead time between cycles.

The switching regulator would overcharge C7 if it was left to oscillate continuously. Instead, it is controlled by the regulator which shuts off the switcher by turning Q13 on. This holds off the base drive to Q16 and thus prevents it from turning on. R49, Q14 and CR42 provide a base drive circuit for Q16. When Q16 is on, the secondary of T3 puts out about 10 V. This turns Q14 on, which sources a heavy current into Q16's base, thereby holding Q16 on.

As Q16 begins to saturate (collector voltage equals base voltage), CR41 begins to conduct and this shunts the base current of Q16 (from R49) through CR41 and through Q16's collector.

An equilibrium point is reached where Q16's base current is just enough to hold Q16 on the verge of saturation. CR37 and CR38 re-

verse bias Q16's base-emitter junction when Q16 shuts off. At that instant T3's secondary voltage is about -6 V, and this pulls the base of Q16 to about -4 V with respect to the emitter. CR42 prevents current from flowing through Q15's base-collector junction during this turn off time.

2.2.5.3 Regulator

The regulator serves two purposes: (1) it prevents the 116 Vdc supply from exceeding about 130 Vdc, and (2) it detects power supply fault conditions.

As a voltage regulator, part of Z2, along with Q2 and Q3, is used to form an amplifier which shuts off the switching regulator when the 116 V supply increases beyond 130 Vdc. R9, 10 and 11 form a voltage divider that reduces the 116 V to about 8.5 V and drives a transistor with a zener (reverse biased base-emitter junction) in series with the emitter.

If the voltage increases, the transistor turns on, and this turns Q2 on. Q2 is current limited to 1 mA by R15, and Q2's collector current flows into Q3's emitter then down through R16 to Q13 which shuts off the switching regulator. (R16 protects the high voltage transistor, Q3, from possible fault conditions.) R14 provides a voltage drop which feeds back through R13 to give positive feedback (hysteresis) to the regulator. In normal operation, the 116 Vdc supply is controlled by Z1 and its associated circuitry.

This results in a control signal to Q13 that lets the switching regulator put out bursts of power by turning on for 5 to 20 power cycles then shutting off for a while. CR2 and CR5 limit the voltages that run the regulator.

The fault detection circuitry of the controller/regulator is quite complex and can best be understood by considering a power turn on situation.

When the mainframe/satellite is switched on, the switching regulator immediately goes into a free-run oscillatory mode which results in a current of about .5 A into C7. This charges at about 5 V/msec. R20 and C3 hold the regulator off during this initial start-up phase.

At voltages below about 100 V, RN1(pins 7-8) holds pin 5 of Z3 low which causes the DISABLE line to go high. This keeps the outputs

of Z4 high and thus the drive to the inverter circuit is kept low. When C7's voltage finally reaches 100 to 105 V, CR8 and RN1 (pins 5-6) overpower RN1 (pins 7-8) and pull pin 5 of Z3 high which causes the disable line to go low.

The oscillator now drives Z4, which drives gates that drive the inverter circuitry. Thus, the inverter does not turn on until the 116 V supply is close to full voltage.

While C7 is charging, so is C2 which turns on Z2 at pin 12. This pulls Z2 pin 6 low and prevents the high DISABLE signal from turning on Q3, thereby shutting down the switching regulator.

When the 116 V is finally attained, Z1, which monitors the 5 Vdc line, assumes control of the switching regulator through R14 and Q3.

If an overload or short circuit condition exists, the inverter draws more than .5 A of current and discharges C7 in spite of the switching regulator's efforts to keep it charged.

When the inverter supply voltage drops to about 90 V, RN1 (pins 7-8) pulls pin 5 of Z3 low which sends the DISABLE line high. This freezes Z4, thereby shutting down the inverter; and also turns on Z2 pin 6 through R19. This transistor overrides Q2 and turns Q3 on, which in turn shuts off the switching regulator.

With the inverter off, the supply voltage for the regulator/controller (normally 6 V) drops; and this, through CR3 and CR4 pulls pin 3 of Z2 low causing that transistor to turn on and therefore Q2 to turn on. The switching regulator is then held off.

To power the supply back up: turn off power; wait 15 seconds for all the capacitors to discharge; then turn the power back on.

In the event of a power line failure the power supply can run the system for a few missing line cycles because of the stored energy in C26 and C27. When their total voltage drops to about 200 V, Q4 is turned on by R45, CR35 and R25 (CR36 normally keeps CR35 back-biased). OC2 turns on which signals the microprocessor that power will soon fail. The DISABLE line is pulled low through CR10 to keep the switching regulator and inverter running for the duration of the loss of power.

2.2.5.4 Oscillator, Driver, and Inverter

The oscillator circuit is a CMOS R-C oscillator that normally free runs at about 26 kHz. This gets divided in half by Z4 which drives the CMOS inverters that drive Q5, 6, 7 and 8. They, in turn, drive the power transistors, Q10 and Q11.

The oscillator can be synchronized at a higher frequency than its free run frequency by driving Z2 pin 9 from pulse transformer T2. In normal operation this driving frequency is 30.72 kHz. This results in a 15.36 kHz drive signal to the inverter.

Z4 drives the Z3 inverters through R-C networks which add about lusec delay to turn on, but zero delay to turn off the power transistors. Thus, when Q10 is turned off, there is about a micro-second of delay before Q11 turns on. This prevents Q10 and Q11 from being on simultaneously.

Diodes CR13 through CR16 form Baker-clamp drive circuits that prevent Q10 and Q11 from saturating when conducting. C10 and C11 are speed up capacitors that result in fast turn-on and turn-off switching. CR18 through CR21 rectify a secondary winding of T1 and provide the 6 V supply used by the control circuitry.

2.2.5.5 Output Rectifiers, Filters, and Regulators

CR22 thru CR25 and CR27 thru CR30 rectify two secondary windings of T1 to give +5, +16, and -16 Vdc. These output lines have LC filters to minimize ripple.

The logic 5 V supply also has over voltage protection (Q12) which shorts the supply if the voltage rises much above 6 V. This overloads the inverter and results in a systematic shut down of the power supply. (This scheme is also known as crowbar protection.)

The output lines phase1 and phase2 are used to drive the FEM's and any option card with an isolated power supply. Since these lines are phase locked to the master oscillator, they can be used for precise timing as well as power applications.

The LOGIC +5V output is filtered by L2 and C17 to form a 5 Vdc supply for the display LEDs. auxiliary +12 and -12 Vdc supplies are obtained from the unregulated +16 and -16 Vdc supplies, respectively, by regulators Z5 and Z6.

The LOGIC +5V output is regulated by Z1, which compares the 5 volt output with a reference voltage from CR1. Z1 drives an opto-isolator, OC1, that controls the regulator, which, in turn, controls the 116 volt line through the switching regulator. Only during start-up or a fault condition does the regulator take control.

2.3 FRONT END MODULE (FEM), GENERAL

The following discussion describes the five basic FEM types. These FEMs, which have many circuits and functions in common, are:

FEM Type	PCB Assy	Mechanical Assy
Solid-state FEM	230-4400-xx	231-5001-xx
Reed Relay FEM	230-4410-xx	231-5002-xx
Current Xmtr FEM	230-4411-xx	231-5002-xx
High Voltage FEM	230-4412-xx	231-5004-xx
RTD FEM	230-4430-xx	231-5010-xx

The FEM is a 20-point multiplexer that drives an analog to pulsewidth converter. Each FEM type consists of a signal conditioner, amplifier, integrator, and zero cross detector. Digital communication to a FEM is serial, using a 16-bit data stream. The FEM's have 22 addressable channels, with programmable gain ranges. The Solid-state and Reed Relay FEM's also have a programmable break detect signal. The RTD FEM is programmable for either three or four wire operation.

A FEM actually converts 22 channels. The first 20 channels are signal input points. The other two channels are a zero channel (for autozero), and a temperature reference diode channel (or autocal for RTD's).

All FEM types share a common analog conversion technique--the Solid-state and relay multiplexers are similar, but warrant separate descriptions. The digital communications circuits are common among all FEMs. The discussion of the digital communications includes some repetition of description from the PIA circuit theory (refer to 2.2.3), since the interface is best understood as an entity.

2.3.1 Analog Conversion Circuits

Figure 2-2 is a block diagram of the analog portion of the solid-state FEM. An input signal is first selected by a multiplexer whose output is selected from a bank of multiplexers by a submultiplexer. This selected signal is filtered, amplified, and then digitized.

The analog to digital converter (A/D) is a dual slope integrating type, with an integrator amplifier whose output drives a zero crossing amplifier. The time at which the zero crossing is detected (output from the zero crossing amplifier) is directly proportional to the analog input voltage.

The input filter is a conventional unity-gain buffer with positive feedback. However, it is utilized in an unconventional manner; the output being taken from the input to the buffer, rather than from the output, in order to avoid voltage drift in the buffer.

The pre-amp normalizes all plus full scale input voltages to +2.2v, and contains noise reduction circuitry that results in converted values stable to within +/- 0.5 microvolt.

The pre-amp output is fed to an integrator with auto-zero circuitry, for low voltage drift, which also stores a negative full scale voltage. Storage of the negative full scale voltage is equivalent to adding a constant voltage to the pre-amp output. This allows a single polarity reference voltage to be used. The single polarity reference eliminates zero gap problems encountered in dual polarity reference voltage techniques.

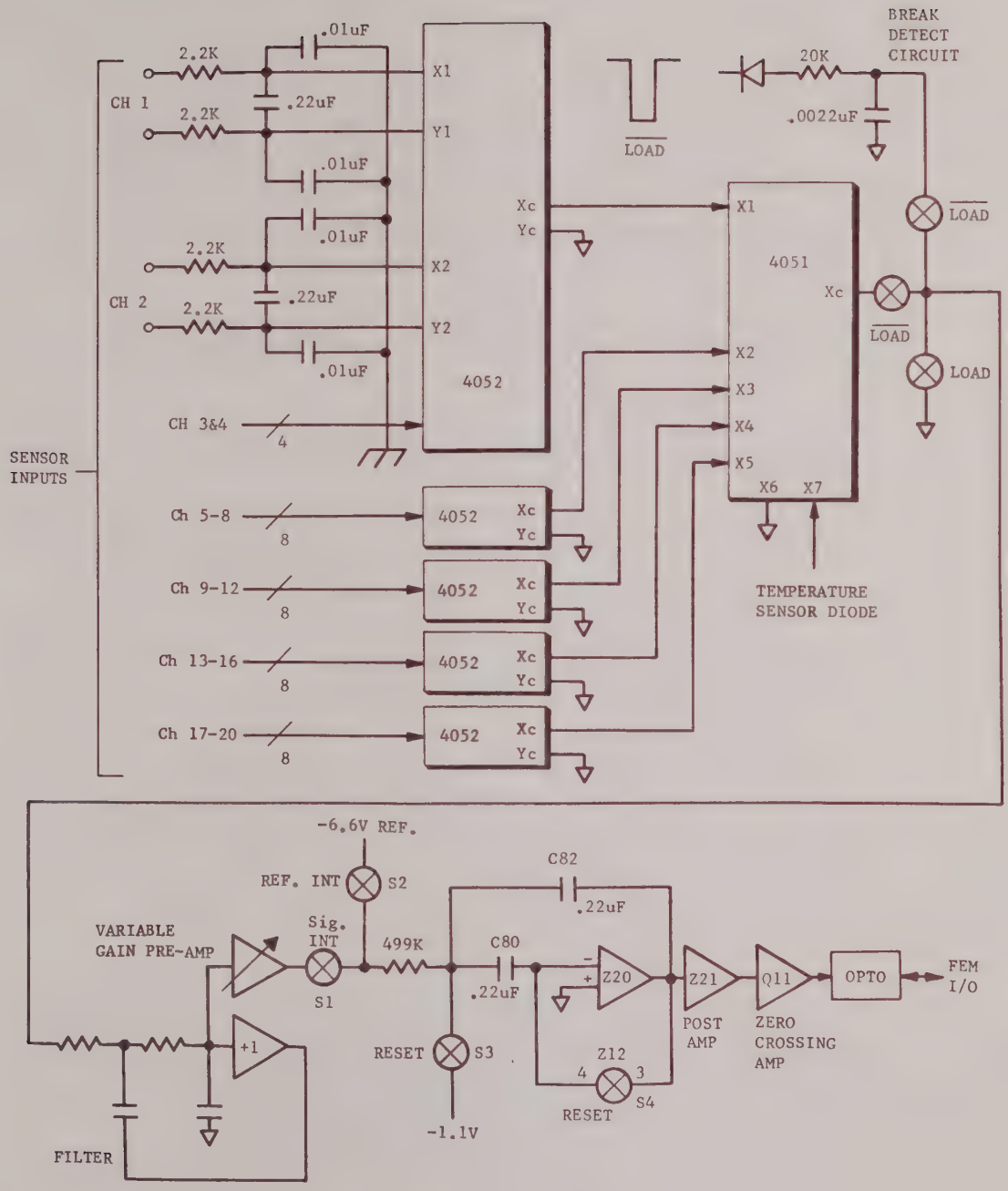


FIGURE 2-2. BLOCK DIAGRAM, SOLID STATE FEM

NOTE

Since the RTD FEM is unipolar, the negative full scale voltage is set at zero volts.

Offset and negative full scale voltage storage is accomplished as follows:

a) During reset, while the input filter and pre-amp are settling to the input voltage, switches S1 and S2 are open; S3 and S4 are closed.

b) Due to feedback action, the input of the integrator is driven to the integrator offset voltage.

c) Since both the input and the output of the integrator are at the integrator offset voltage, both C80 and C82 are charged to -1.1v plus the integrator offset voltage (zero volts instead of -1.1 for the RTD FEM).

d) When reset terminates and signal integrate starts, S3 and S4 open, S1 closes, and S2 remains open.

e) The pre-amp will try to drive the summing junction positive through the 500k ohm resistor. The integrator input terminal now sees a voltage equal to its offset voltage plus a small error voltage. By definition the integrator interprets the offset voltage as zero and responds only to the error voltage. The integrator will drive the summing junction (the junction of the two capacitors) to -1.1v, since C80 and C82 are both charged to -1.1v (zero volts for the RTD FEM).

f) The integrator output will move negative in a ramp-like fashion (see Figure 2-3), feeding back a correction voltage to maintain the summing junction at -1.1v. As a result, a current flows through the 500k ohm resistor proportional to the pre-amp output plus 1.1v. This current charges C82. Because the integrator is an FET input amplifier with very high input resistance, C80 will not discharge.

g) The integrate cycle ends (100ms); S1 opens and S2 closes.

h) The -6.6v reference will try to drive the summing junction negative through the 500k ohm resistor. The integrator output will now ramp positive. C82 will be charged by a current through the 500k ohm resistor determined by -6.6v plus 1.1v.

i) The integrator output will go from a negative voltage, caused by the input, toward zero, driven by the reference. When the voltage reaches zero, the post-amp and zero-crossing amplifier will transmit a pulse to the mainframe.

Figure 2-3 illustrates the integrator output and gives the pertinent equations for the signal integrate and reference integrate cycles. Solving the two expressions for -v gives:

$-v = T1(Ex+1.1)/RC4$ and $-v=T2(6.6-1.1)/RC4$

equating: $T1(Ex+1.1)/RC4=T2\ 5.5/RC4$

produces $T2=T1(Ex+1.1)/5.5$ for all FEMs except
$T2=T1(Ex)/6.6$ for the RTD FEM

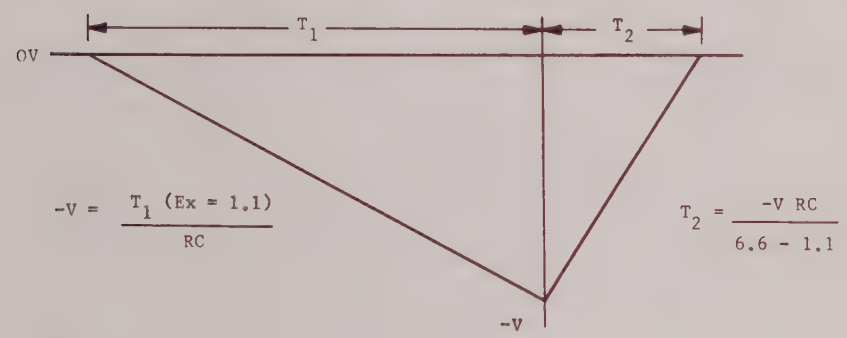


FIGURE 2-3. INTEGRATOR OUTPUT

This equation for the input transfer function is converted by software into a signed decimal number, and assigned engineering units. The software periodically takes a reading with Ex forced to zero and stores this value. When each input reading is taken the stored value is subtracted.

2.3.2 Solid-state Multiplexer

The Solid-state Multiplexer (mux) utilizes CMOS switches (Z1-Z5) for selecting the desired input channel. Figure 2-2 shows the in-

put filtering for two channels (in the actual circuit all channels have input filters). These input filters are necessary to reduce RFI currents, which, if not filtered out, would be partially rectified by the analog input circuitry and show up as microvolt level signals (0 to 100 microvolts). The .01 uf capacitors return RFI currents to the chassis and minimize their effect.

The CMOS switches used are 4052 dual 4-channel multiplexers selected for their low leakage and low offset voltage. Both high and low leads are switched for differential channel selection. The 4052 outputs are sub-multiplexed by Z7 (a 1-of-8 mux chip). Sub-multiplexing reduces, by five, leakage current effects, for increased accuracy when measuring microvolt level signals.

The sub-multiplexer also selects zero volts as an input, or the temperature sensor diode for thermocouple compensation. The zero volt input is utilized, as previously mentioned, for software conversion of the offset transfer function to a bi-polar transfer function.

The selected input voltage is gated by additional switches (Z6) to minimize the effects of channel address changing (during this time the input is grounded), and to introduce a break detect signal.

Break detect is accomplished by charging capacitor C64 during channel selection via Q14, and then discharging C64 through the selected channel source resistance. In the event of a break, the channel will not discharge the capacitor, and a reading of negative overload will result.

2.3.3 Reed Relay Multiplexer

The relay mux circuitry (see Figure 2-4) is nearly identical to the solid-state mux. The obvious exception is the fact that relays are used for channel selection instead of CMOS switches. Additional differences are in the configuration of the RFI filters and the absence of a sub-multiplexer chip.

The RFI filter for the relay mux is configured differently for two reasons: First, the relay contacts will not rectify, so a common differential capacitor can be used; second, large common mode voltages are anticipated in the relay mux, so smaller per channel capacitors are necessary to keep common mode currents to earth within limits.

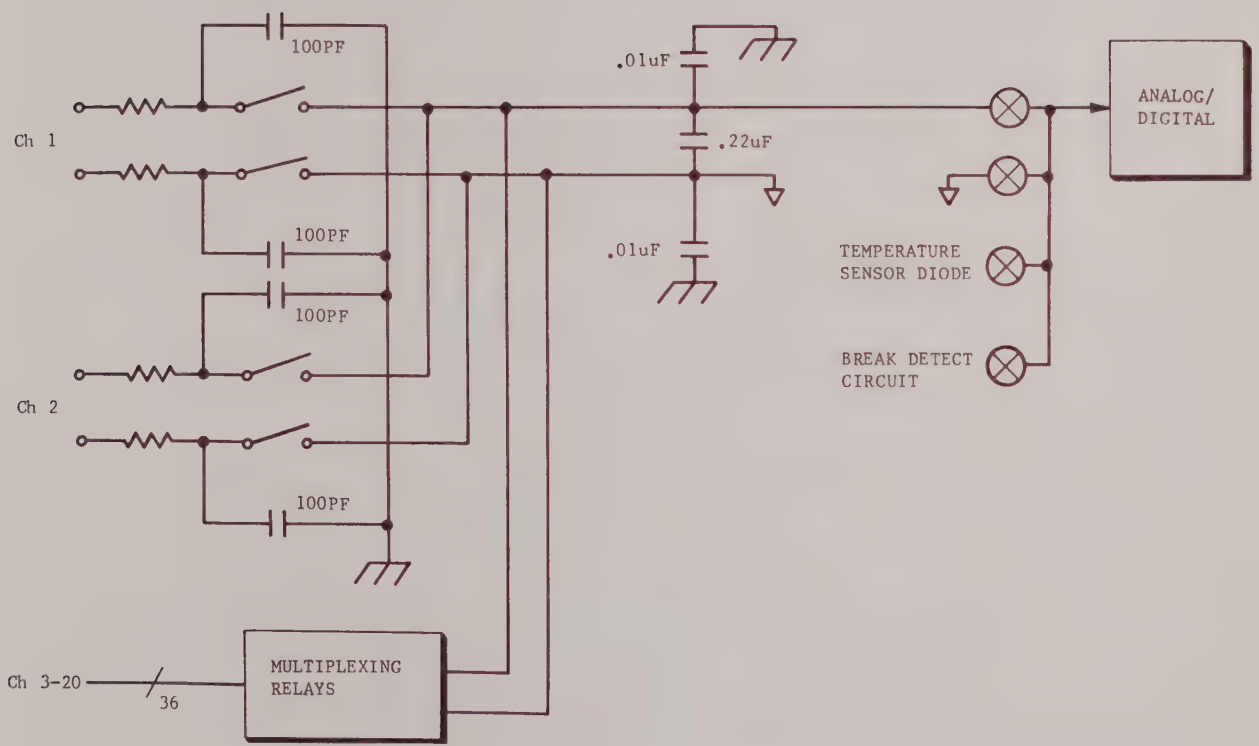


FIGURE 2-4. BLOCK DIAGRAM, REED RELAY MULTIPLEXER

2.3.4 RTD Multiplexer

The RTD mux is very similar to the Solid-state mux; the voltage leads being scanned identically. However, a floating current source has been added, the minus full scale voltage is no longer stored on the integrator capacitor, and the A/D reference is derived from the floating current source.

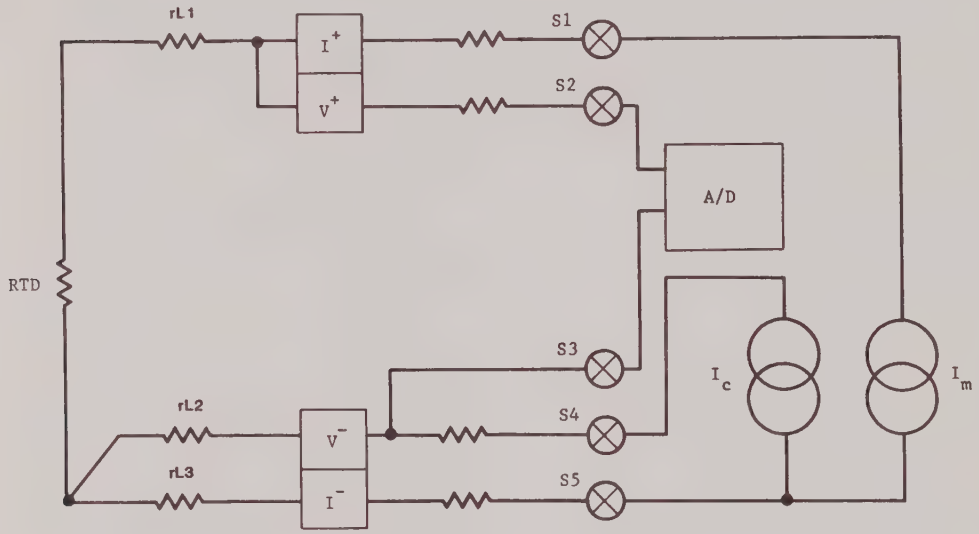


FIGURE 2-5. THREE-WIRE RTD CONFIGURATION, ONE CHANNEL

Figure 2-5 shows one channel of the RTD mux and illustrates the measurement principles involved. A floating current generator (derived from an independent transformer winding on the power transformer) drives a current Im through S1 and S5 to create a voltage drop across the RTD. Switches S2 and S3 connect the RTD, as a voltage source, to the A/D converter. The A/D input voltage is proportional to the RTD resistance.

The additional current generator, Ic, and the switch S4 are included to compensate voltage drops in the RTD interconnect leads. With Ic "off", the voltage sensed by S2 and S3 includes a drop Imrl. There is no contribution due to rL2 or rL3 since no current flows in rL2, which is connected to the high input impedance A/D, and S3 senses the voltage before the drop in rL3.

With Ic "on", an additional term -IcrL2 is added to the voltage sensed by S2 and S3. Since the lead resistance rL1, and rL2 are nearly equal; making Ic equal to Im eliminates lead resistance errors. However, if rL1 and rL2 errors must be completely eliminated, this can be done by adding a fourth wire from the top of the RTD to V+. In addition, the jumper from V+ to I+ must be removed, and Ic turned off. Under these conditions S2 and S3 will sense the voltage across the RTD without any contribution due to rL1 and rL2.

Figure 2-6 shows the current generator switching utilized in the RTD mux. During reset and signal integrate, the current Im is switched through the selected RTD. During reference integrate all switches are off except SR1, SR2, and SR3. The current Im flows through Rref and forms a Thevenin equivalent of a battery with an output voltage ImRref and a source resistance Rref. The positive terminal of this voltage is grounded by SR2; this voltage then becomes a negative reference.

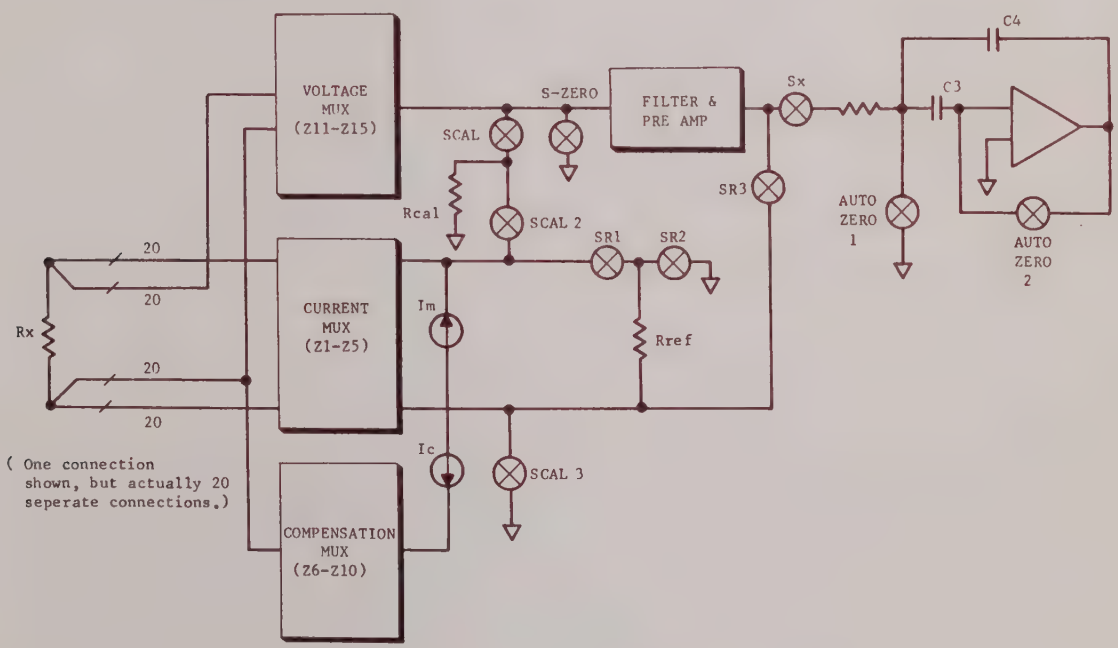


FIGURE 2-6. RTD MULTIPLEXER CURRENT GENERATOR SWITCHING

Since the same current excites the RTD and produces the reference voltage, it does not have to be a precision current. The current appears in both numerator and denominator of the transfer function and cancels. To further increase the accuracy of measurement, calibration resistor Rcal is included.

During reset and signal integrate, the current Im is switched through Rcal if the RTD mux is addressing the autocal channel. The calibrate resistor is thus measured and the resultant reading stored for scale factor correction.

Similarly, the switch S-zero grounds the input for a zero reading, and a correction factor for zero is stored. With these two measurements the RTD mux can automatically calibrate itself.

Since the RTD measurement voltage is unipolar, it is not necessary to add a constant to the input voltage. The switch S-autozero is connected to ground, and the only voltage stored on the capacitors is the integrator offset voltage, which is thereby autozeroed out.

2.3.5 Digital Communication

The communication link to the analog module is two twisted pairs in a foil shield. One pair is driven by a 15 kHz square wave that provides power to the analog module and a clock for timing in the analog module. The other pair is a bi-directional link which transmits a convert start pulse string to the analog module and receives a convert complete pulse from the analog module.

The convert start pulse is the first of 16 pulses that transmit instructions to the analog module in a serial mode. Contained in this serial pulse string is: channel address, break detect enable or 4 wire enable, and gain selection.

Figure 2-7 is a block diagram of the data receiver scheme of the analog module. The D input of the shift register is driven from a 15 kHz square wave which represents alternate "ones" and "zeroes". The shift register is clocked by the data, shifting "ones" or "zeroes" depending on the state of the 15 kHz clock as the data clocks the shift register. Since the shift register is 8 bits long, only the last 8 bits transmitted are retained in the register.

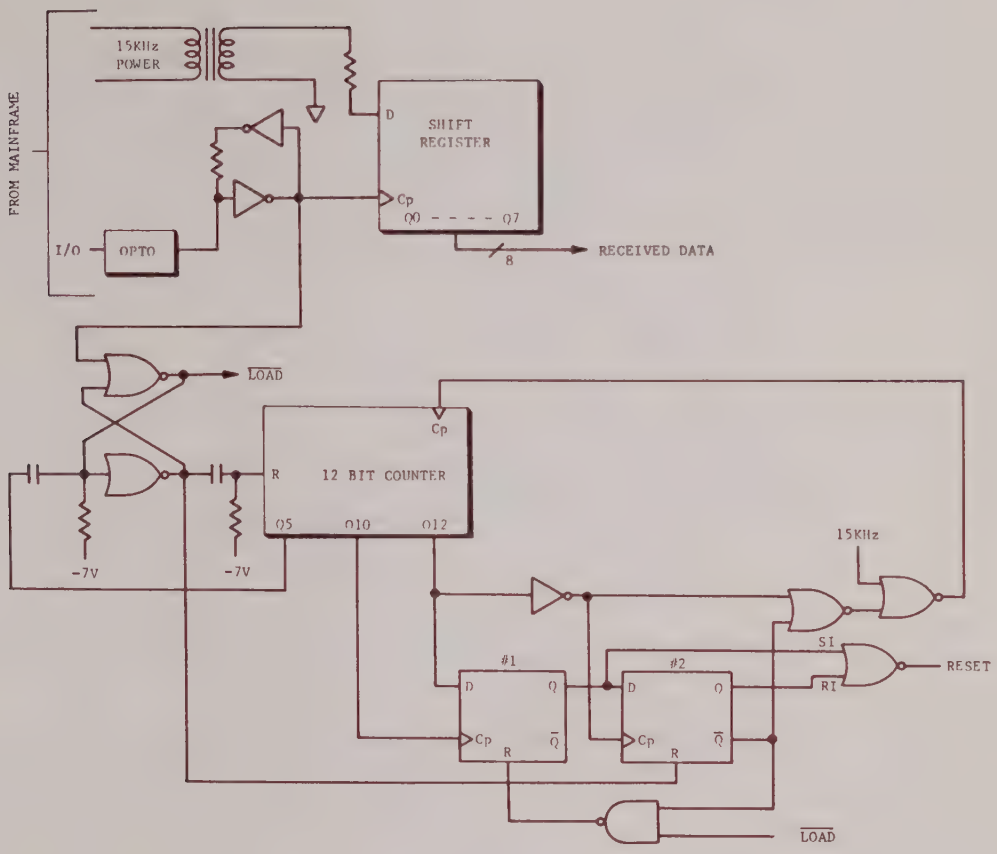


FIGURE 2-7. BLOCK DIAGRAM, DATA RECEIVE/DECODE CIRCUITS (FEM)

When the first pulse is transmitted a counter on the PIA board or Satellite Controller board is started. Similarly, when the first pulse is received by the analog module, a counter is started in the FEM. Both counters are counting the same 15 kHz square waves so synchronization is established.

The eight bits retained will be decoded as shown:

G1	G2	BD	C	B	A	B'	A'
last bit							first bit

Channel address bit weights are: A'=1 B'=2 A=4 B=8 C=16

When Break Detect bit BD is set low (0), an open circuit at the input will cause a negative overload.

Voltage/Thermocouple FEM

When Gain bit G1 =	0	0	1	1
and, Gain bit G2 =	0	1	0	1
then Gain Range =	20mv	80mv	400mv	2volt

RTD FEM

When Gain bit G1 =	0	0	1	1
and, Gain bit G2 =	0	1	0	1
then resistance =	230ohms	390ohms	650ohms	not used

The channel number is given by the binary number +1 formed by CBAB'A'.

Channels 21-24 are ZERO
Channels 25-28 are:
Volt/TC FEM: Temp Reference Diode
RTD FEM: 225ohm autocal resistor

The FEM data must be re-mapped for proper transmission. The data is transmitted PA7 first and PA0 last (mainframe) or D7 first and D0 last (satellite). However, the received data is interpreted with the first received bit as the LSB. The consequence of this is that the transmitted data must be loaded as shown:

PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0 (mainframe)
D7	D6	D5	D4	D3	D2	D1	D0 (satellite)
A'	B'	A	B	C	BD	G2	G1

The data to be output is sent via a PIA on the mainframe PIA board or via RAM memory on the Satellite Controller board. The data is output in two bytes. These two bytes are loaded into shift registers selected by the PB6 and PB7 lines of the PIA B register (mainframe) or LD1(not) LD2(not) lines of the Satellite Controller board. A 15 Hz signal initiates communication.

Figure 2-8 is a block diagram of the bit stream encoding circuit on the PIA board and Satellite Controller board. The negative transition of 15 Hz sets a flip-flop which opens a pulse gate, and causes the contents of a 16-bit shift register to be serially transmitted at a 15 kHz rate. Data is output in an encoded form with positive output transitions from the shift register determining "1"s and "0"s in conjunction with the logic state of the 15 kHz clock at the moment of transition.

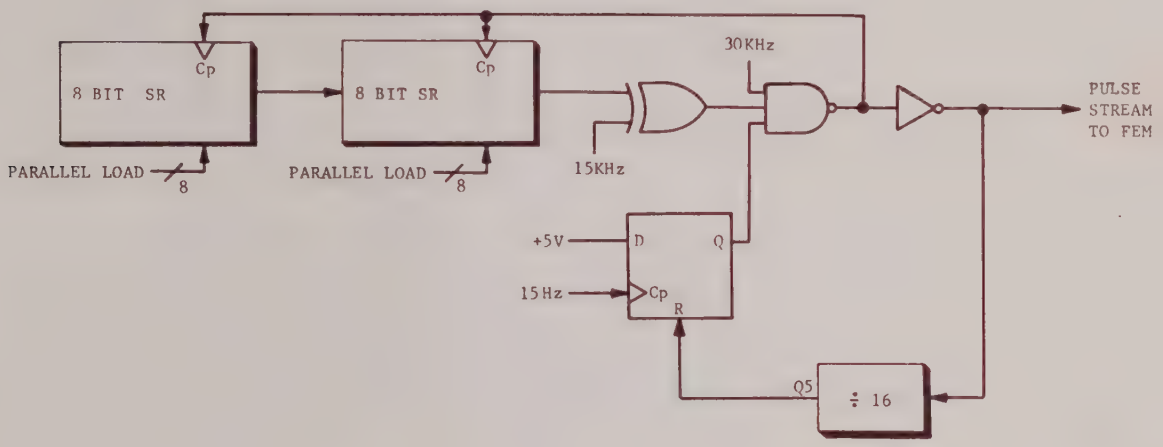


FIGURE 2-8. BLOCK DIAGRAM, DATA SHIFT/ENCODE CIRCUITS (PIA/SAT PCBs)

The data is encoded by an Exclusive-OR gate, and the 30 kHz clock, which forces positive transitions to occur at the center of the 15 kHz high or low state. The Exclusive-OR gate compares the shift register output to the 15 kHz clock and inhibits negative transitions when they are the same. Since the output is held high there is no positive edge, with the net result that positive transitions occur only during the 15 kHz state opposite from the data. Decoding is done by using the positive edge to strobe the opposite phase of 15 kHz into a shift register.

Figure 2-1 shows pertinent waveforms for encoding serial transmission of Channel 6 in the 2 volt range. Notice that the first 8 bits transmitted are "1"s followed by the data. The receiver only retains the last 8 bits transmitted, so these bits serve only to notify that data transmission is starting.

The encoded bit stream is counted by a binary counter. When 16 bits have been transmitted, the Q5 output of the counter resets the flip-flop, which in turn shuts off a pulse gate, and the system waits for the return of the zero crossing.

The bit stream is generated on the PIA board or satellite controller board, and is directed to a 4051 1-of-8 multiplexer that drives the output line directly.

Figure 2-9 illustrates one channel of the transmitter-receiver pair. The TTL output drives the FEM input line directly, and the pulse is coupled to the FEM through a 220 ohm resistor on the FEM card which may be selected by connecting to the appropriate input pins on the FEM.

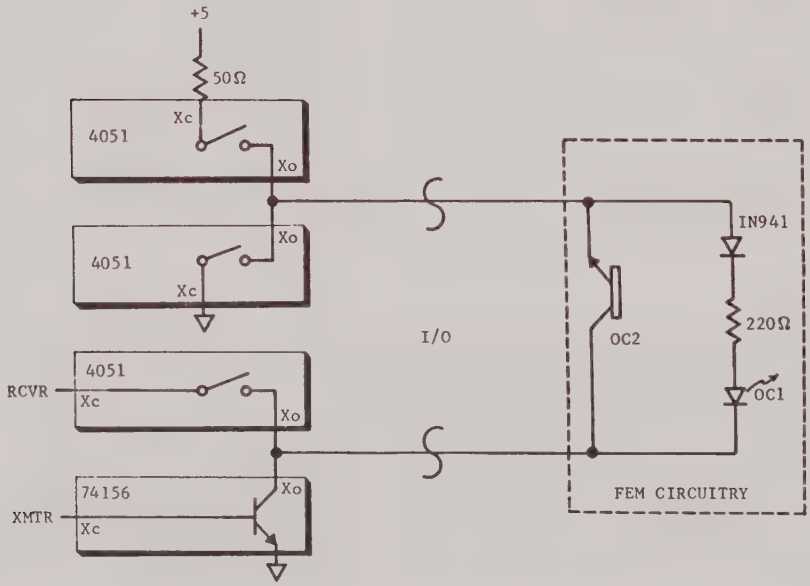


FIGURE 2-9. TRANSMITTER/RECEIVER PAIR--MAINFRAME/SATELLITE

The zero crossing comes back over the same line used for bit transmission. When the zero crossing occurs, transistor OC2 turns on, which causes an inverter turn off. The polarity of the lines are reversed during data reception, utilizing the top multiplexer

which switches that line from +5v to ground. The high state of the inverted received signal is clocked by the 1 MHz system clock into a flip-flop, and strobes the system counter contents into a register.

Since this counter originated the conversion when its content was zero, the present content is a direct measure of the elapsed time from convert start. The dual slope converter generates a time proportional to the analog input, so the counter contains a number directly proportional to the analog input.

2.3.6 FEM Timing

The basic conversion time for each front end module is 333 1/3 ms. This time is divided into intervals of 166 2/3 ms, 100 ms, and 66 2/3 ms as shown in Figure 2-11 below.

During the first nominal 1 ms the channel input is opened and the A/D input is grounded. This is the time that the 16 clock pulses are shifting data through the shift register. After this time the input signal is switched through the multiplexer to the A/D input filter and pre-amp. The input filter and pre-amp are allowed the remaining 166 2/3 ms (less the nominal 1ms) for settling to the input voltage.

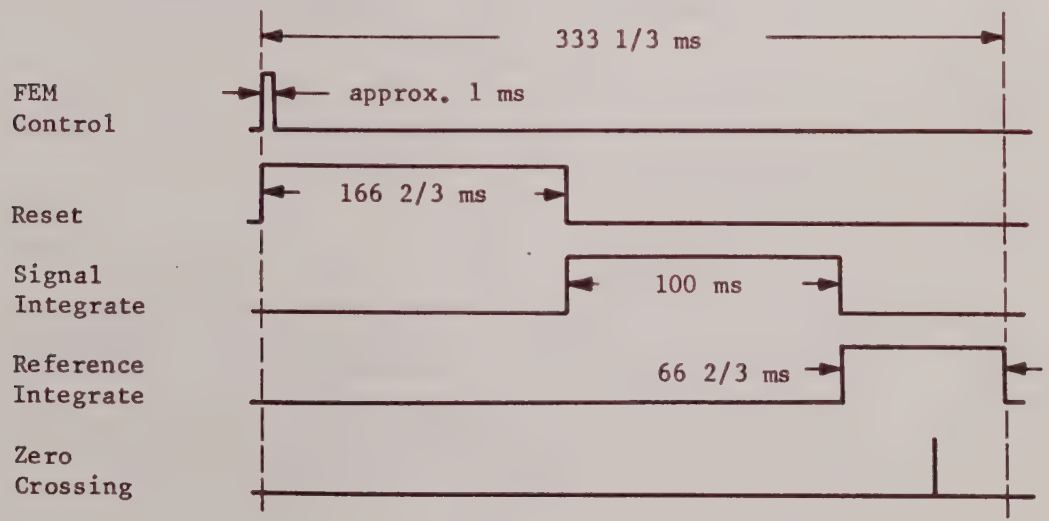


FIGURE 2-10. TIMING DIAGRAM, BASIC CONVERSION CYCLE

The FEM timing waveforms are derived from the logic shown in Figure 2-7. When a FEM receives the bit stream (from either the PIA board or Satellite Controller board), an RS latch formed by two cross-coupled NOR gates is set.

Setting the latch resets all the logic. The counter is reset by the transition through an RC network and, the two D flip-flops are directly reset. The 12 bit counter counts 15 kHz derived from the mainframe. After 16 counts, the Q5 output goes high, and the RS latch is reset.

The counter continues to count; when Q12 goes high and Q10 makes a positive transition, D flip-flop #1 is set. This occurs after 2560 counts, or 166 2/3 ms (the clock is slightly faster than 15 kHz). Setting flip-flop #1 causes signal integrate (SI) to go TRUE, and RESET to go false (since RESET is the NOR of SI and RI).

When Q12 then goes low, flip-flop #2 is set, which resets flip flop #1 through a NAND gate. This causes reference integrate (RI) to go high, and SI to be terminated. This occurs after 4096 counts, or 266 2/3 ms.

Signal Integrate time is thus 100 ms (266 2/3 ms - 166 2/3 ms). If the counter continued to count until Q12 went low, the NOR gate monitoring RI(not) and Q12(not) would shut off the 15 kHz clock gate and stop counting--waiting for the next bit stream. This would occur after 6144 counts or 400 ms. However, the FEM normally receives bit streams every 333 1/3 ms, so this state is not reached.

The conversion timing of the FEMs is interlaced so that each one starts a conversion every 66 2/3 ms.

2.3.7 System Algorithm

The mainframe/satellite data output is derived by digitizing the zero point and storing that value (ZERO). Subsequent conversions subtract ZERO from the A/D counts. The ZERO reading for any range must be read with the corresponding gain bits set for that range. The algorithm for all FEM's except an RTD FEM is:

$$R = Rn - ZERO$$

Where:
R is the compensated output counts
Rn is the counts measured on point n
ZERO is the counts measured with zero input
ZERO = 20879 +/- 400 counts (same gain as Rn)

For an RTD FEM the counts must be multiplied by an autocal constant in addition to subtracting ZERO. The algorithm for the RTD FEM output is:

$$R = (Rn - ZERO)(CORRECT)/(CAL - ZERO)$$

Where:
R is the compensated output counts
Rn is the counts measured on point n
ZERO is the counts measured with zero input
ZERO = 300 +/- 50 counts (same gain as Rn)
CORRECT is the correct counts for 225 ohms
CAL is the counts measured for 225 ohms

230 ohm range CORRECT = 64,110
390 ohm range CORRECT = 37,809
650 ohm range CORRECT = 22,500

2.4 SATELLITE BOARDS, GENERAL

The two basic board assemblies used in the satellite unit are (1) the Satellite Controller board, and (2) Power Supply. The mainframe and satellite units use the same power supply and FEMs. Since these have already been discussed, the satellite controller board is the topic of the following discussion.

2.4.1 Satellite Controller Board

Assembly: 244-4310-xx
Schematic: 244-6310-xx

The main circuit areas of the Satellite Controller Board are:

1. MPU
2. SERIAL I/O
3. MEMORY
4. FEM INTERFACE CIRCUITRY
5. SYNCHRONOUS RESET CIRCUITRY

2.4.1.1 MPU

MPU 4F is an 8-bit Motorola 6803 microprocessor. (See page 1 of schematic.) This device uses a multiplexed data bus with the lower order address appearing on the data bus when the address latch enable signal at 4F pin 39 goes high. The basic function of the MPU is to establish communication between the mainframe and the FEMs within the satellite.

2.4.1.2 Serial I/O

Serial communication between mainframe and satellite is over standard full duplex 20 mA current loops. (See page 2 of schematic.) The transmit and receive loops are opto-coupled to the satellite controller MPU (transmitted data from 4F pin 12 and received data to 4F pin 11). The transmit loop gives data such as RESET status and raw A/D counts derived from the FEM inputs to the mainframe. The receive loop takes FEM configuration information from the mainframe to the satellite MPU.

The serial clock generator circuit determines the speed of serial data communication (baud rate). The heart of this circuit is vol-

tage controlled oscillator 4J. The 153.6 kHz output frequency at 4J pin 4 is divided down by counter 5K. The various counter outputs are switch selectable for input to MPU 4F pin 10. The baud rate switch selection is set at the factory for 4800 baud.

2.4.1.3 Memory

A 2K x 8 RAM (4A) stores the data received from MPU 4F. (See page 1 of schematic.) This data includes FEM configuration data and point skip status. There are provisions for RAM expansion for extra operation features planned in the future. A particular RAM is selected by decoder 3D from address lines A13-A15.

A 2K x 8 EPROM (4C) stores the satellite's operating program. The program performs internal configuration of the MPU and generates timing signals.

2.4.1.4 FEM Interface Circuitry

The operation of the satellite controller board's FEM interface circuits (page 2 of schematic) follow the same basic principles as outlined in the PIA board description of the same function. (Please refer to 2.2.3.1 through 2.2.3.3.) The major differences in the satellite controller's FEM Interface circuitry are (1) FEM data is loaded from RAM rather than a PIA, (2) internal MPU counters are used for the free-running A/D counters rather than external discrete counters, (3) an overrange or open input is detected by the OVR(not) signal clearing the flip-flop rather than the f17 transition clearing the flip-flop, and (4) the FEM transmit and receive loops are connected to a particular FEM by hardware rather than software, using register 1C as follows:

ADDRESS CODE			FEM NUMBER	
1C pin 4 TAC0	1C pin 5 TAC1	1C pin 12 TAC2	transmit loop	receive loop
0	0	0	1st FEM	5th FEM
0	0	1	2nd FEM	1st FEM
0	1	0	3rd FEM	2nd FEM
0	1	1	4th FEM	3rd FEM
1	0	0	5th FEM	4th FEM

Note that the TACx lines are basically vector addresses for the FEM transmit loop. A particular combination of TACx lines provides a corresponding RACx line which addresses the receive loop of a FEM as shown in the table above.

2.4.1.5 Synchronous Reset Circuitry

This functional block consists of logic circuits that output the following signals:

RST(not): resets the MPU when low.

NMI(not): non-maskable interrupt which coincides with counter timer step zero.

TGS: Timing Generator Sync -- a high going pulse during count zero. This synchronizing signal ensures that the external 8-bit Timing Generator Counter is in step with the least significant 8 bits of the A/D counter internal to the MPU. TGS is also high during reset time.

OVR(not): Forces a zero crossing edge signal (ZXE) to latch the zero count if a zero cross is not detected in the allotted time. This is how an overrange or no FEM condition is detected. OVR(not) is normally high, going low only during count zero. It stays high during reset time.

PSYN: A 30.72 kHz signal used to synchronize the power supply so that it can be used for Rx decode clock in the FEMs.

Inputs to the Synchronous Reset Circuitry are:

TBCLR: Tx Bit Count Clear -- a high going pulse output from MPU 4F pin 13 in response to IRQ2 generated by count compare at 8000hex.

DOG: Watchdog Timer Re-trigger -- A pulse output from MPU 4F pin 20 which re-triggers the watchdog timer one-shot. The pulse output is a high going pulse at about 66 msec intervals. If the interval exceeds 150 msec, the watchdog timer times out to force an MPU reset.

FSM: Full Scale Match -- A low to high pulse from MPU 4F pin 9 in response to MPU A/D counter reaching count FFFEhex. The FSM pulse occurs one count later at FFFFhex.

PHZ1: A signal developed from the 15 kHz power supply indicating its polarity. It is used as the Tx encoding clock.

3KH: A 3.84 kHz signal from 2G pin 8 which ensures repetitive resets if DOG is not pulsed.

ECLK: The E-clock or MPU "E". Reset ends in sync with ECLK.

2.4.1.5.1 Watchdog

The watchdog circuit monitors operation of the satellite controller's MPU by monitoring the DOG signal which occurs about every 66 msec from MPU 4F pin 20. (See page 1 of schematic.) Abnormal operation of the MPU interrupts the periodic DOG signal that normally keeps one-shot 3G input pin 12 from timing out. Without the DOG signal, this one-shot times out, and the low level Q output from 3G pin 10 drives the Q(not) output of 3G pin 7 high, which in turn clears one-shot 2H pin 5 low. This drives the Q(not) output at 2H pin 8 high which sinks the +5 V sitting on the MPU's RST(not) line by turning transistor Q1 on. The reset MPU will be initialized in an attempt to recover from the fault condition. The watchdog reset of the satellite MPU is conveyed to the mainframe where it is recorded as an error condition.

2.4.1.5.2 Power-on Reset

The MPU requires a reset as power is applied in order to ensure synchronization. In order to do this, the power voltage rise is capacitively coupled by capacitor C4. The resulting pulse is inverted at inverter 4H pin 8 which forces the Q(not) output of flip-flop 2H pin 8 high. This drives the RST(not) line low by turning transistor Q1 on.

2.5 OPTION BOARD ASSEMBLIES

2.5.1 Alarm Relay Driver Board, General

Assembly: 231-4360-xx
Schematic: 231-6360-xx

The Alarm Relay Driver board has two basic functions:

1. Drive Alarm Relay Panel relays or other other external circuitry.

2. Read the encoded data coming from the key encoder located on the Alarm Relay panel.

The Alarm Relay Driver board is designed to drive two separate Alarm Relay Panels (or other external alarm circuits) and to accept encoded data from both Relay panels. Basically, this board contains the control logic for relay control and data input.

The Alarm Relay Driver board can be broken down into five functional sections:

1. BUS BUFFERS
2. DECODING CIRCUITS
3. TIMING CIRCUITS
4. OUTPUT REGISTERS AND OPTO-ISOLATORS
5. INPUT DATA SYSTEM AND CONTROL

2.5.1.1 Bus Buffers

The Alarm Relay Driver board interfaces to the system bus through bus buffers. The address lines A0 through A15, (not)VMA, and F1x8 are buffered by low power schottky TTL inverters.

The control and timing lines F1, R/W, (not)WPRO, and (not)RESET are buffered by an 8T97 driver, IC 5A. The (not)IRQ line is driven onto the system bus by transistor Q6.

The bi-directional data lines, D0 through D7, are buffered from the system data bus, and driven to the system data bus, by a low power schottky TTL, bi-directional bus buffer, IC 1A.

The direction of the data transfer is controlled by the BR/(not)W line, which is inverted by IC 3Bb, and then used to drive the DIR input of data buffer 1A.

When the BR/(not)W line is logic low, the bi-directional data buffer, 1A, is set to transfer data from the system data bus onto the Alarm Relay Driver board's internal data bus lines, BD0-BD7.

When the BR/(not)W line is logic high, the bi-directional data buffer, 1A, is set to transfer data from the Alarm Relay Driver board's internal data bus lines to the system data bus.

The bi-directional data buffer, 1A, is a tri-state buffer. It's outputs are enabled whenever the (not)EDB line (refer to DECODING CIRCUITS) is logic low.

2.5.1.2 Decoding Circuits

The board select decoding is done by 4B, 5Ec, and 4Af. When (not)BA12, (not)BA14, (not)BA15, BVMA, (not)BRESET, and @M (refer to TIMING) are logic high, and (not)BA11 and (not)BA13 are logic low, the board select, (not)BOARD, line will go to a logic low.

The UA0, Unit Addressed Output, line is decoded by ICs 3Ba, 3Bc, 4Aa, and 4Dc. The UA0 line will go to a logic low when address lines (not)BA4, (not)BA5, (not)BA6, (not)BA7, (not)BA8, (not)BA9, and (not)BA10 are all logic low.

The (not)SW signal is used to select the memory map position of the relay outputs and keyboard input of the Alarm Relay Driver board. The SW signal is generated by switch S3, section C1. It is then inverted by IC 5Ed, forming the (not)SW line.

The A3A line is an altered address 3 line. It is generated by exclusive ORing (not)BA3 with (not)SW, using IC 5Ea. If (not)SW is low, A3A will be logic high when (not)BA3 is logic high. If (not)SW is high, A3A will be logic high when (not)BA3 is logic low.

The (not)EDB, Enable Data Buffer, line will be logic low whenever data is to be transferred to, or from, the Alarm Relay Driver board. The (not)EDB line controls the tri-state outputs of the bi-directional data buffer, 1A. The (not)EDB line is generated by decoding circuitry consisting of 4Ca, 5Bb, 4Ea, 4Eb, 4Ec, and 4Fa.

The UA0 line is NORed with the (not)BA10 line by IC 4Ca. The resulting signal is NANDed with the A3A line and the inversion of the (not)BOARD line by NAND gate 4Eb. The (not)BOARD line is inverted by IC 4Cd.

The output of 4Ca is inverted by the exclusive OR gate 5Eb, then NANDed with the inversion of the (not)BOARD line and the (not)SW line by NAND gate 4Ec. The output of 4Ec is NANDed with the output of 4Eb by NAND gate 4Fa. The resulting signal is NANDed with the system clock BF1 by NAND gate 4Ea. The output of 4Ea is the (not)EDB signal.

The output data register strobes, CK0 through CK3, are used to select which of the four output data registers (refer to OUTPUT REGISTERS AND OPTO-ISOLATORS) is to be written to. The strobes are generated by IC's 3C and 3D.

Address lines (not)BA0, (not)BA1, and (not)BA2 are used as select inputs to the 1-of-8 decoder, IC 3C. The (not)BOARD line acts as one logic low enable to 3C and the UA0 line acts as the other logic low enable. The A3A line acts as the logic high enable for 3C.

When (not)BOARD and UA0 are both logic low in conjunction with A3A being logic high, the output of 3C, as selected by the (not)BA0, (not)BA1, and (not)BA2 address lines, will be enabled. The selected output will go to a logic low. The output-data-register select lines come out on the Y4, Y5, Y6, or Y7 outputs of 3C.

The Y7 output is NORed with the BR/(not)W signal, by IC 3Da, to generate output-data-register strobe CK0. The Y6 output is NORed with the BR/(not)W signal, by IC 3Db, to generate output-data-register strobe CK1. The Y5 output is NORed with the BR/(not)W signal, by IC 3Dc, to generate output-data-register strobe CK2. The Y4 output is NORed with the BR/(not)W signal, by IC 3Dd, to generate output-data-register strobe CK3.

The Y0 output of 3C is used by the input data control system to generate the RDKY(not) line (refer to INPUT DATA SYSTEM AND CONTROL).

2.5.1.3 Timing Circuits

The system clocks, BF1 and BF1x8, are used by IC 5C to generate a precessed clock. This clock is NANDed with the BR/(not)W signal by NAND gate 4Fc to form the @M clock.

2.5.1.4 Output Registers and Opto-isolators

The Alarm Relay Driver board is designed to drive two Alarm Relay Panels. There are two separate output sections, each having two 8-bit output data registers and eight dual opto-isolators.

The two 8-bit output data registers, 3H and 4H, along with the eight dual opto-isolators, 3KA, 3KB, 3LA, 3LB, 4KA, 4KB, 4LA, and 4LB, and NAND gates 3Eb and 3Ed make up output section A.

The two 8-bit output data registers, 1H and 2H, along with the eight dual opto-isolators, 1KA, 1KB, 1LA, 1LB, 2KA, 2KB, 2LA, and 2LB, and NAND gates 3Ea and 3Ec make up output section B.

The output-data-register strobes, CK0 - CK3, are used to strobe the output data into the respective output register. The output strobes are NANDed with the precessed clock, @m. The output registers hold the data being sent to the relay board via the opto-isolators.

The resistor networks, RN4 - RN7, act as current limiting resistors for the LED (Light Emitting Diodes) in the opto-isolators. The outputs of the section A opto-isolators are interfaced to the external Relay panel via connector J2. The outputs of the section B opto-isolators are interfaced to the external Relay panel via connector J1.

2.5.1.5 Input Data System and Control

The data coming from the Alarm Relay Panel is buffered by opto-isolators and then passed through tri-state drivers onto the on-board input data bus.

The keyboard strobes coming from the Alarm Relay Panel are sent to an arbitration circuit which will decide which keyboard's input data will be enabled onto the input data bus, and then strobed into the input data register.

Opto-isolator 1MB buffers the data STROBE(not) and data STROBE ENable coming from Relay panel B.

Opto-isolators 1MA and 2MB buffer the data coming from relay panel B.

Opto-isolator 2MA buffers the data STROBE(not) and data STROBE ENable coming from Relay panel A.

Opto-isolators 3MA and 3MB buffer the data coming from relay panel A.

To prevent noise on the interface cable, between the Alarm Relay Driver board and the Relay panel, from getting into the Alarm Relay Driver board's input data system, the outputs of the opto-isolators are fed into schmitt-trigger inverters.

The received data is buffered by a tri-state buffer, 5J, onto the onboard input data bus. The data is then strobed into the data register, 5H, under the control of the keyboard arbitrator circuitry, for transfer to the system bus through the system bus driver 1A.

The keyboard arbitrator circuit decides the order in which the Relay panel's keyboard input data is read by the Alarm Relay Driver board. The keyboard arbitrator consists of IC's 5K, 5L, 5M, and 5N.

If the keyboard input data from Relay panel B, J1, should become active, the STROBE EN signal will be logic high and STROBE(not) will go to a logic low state. These two signals are buffered by opto-isolator 1MB. The logic high STROBE EN signal will cause the output of the schmitt-trigger inverter 4Nf to be logic low. The logic low STROBE(not) signal will cause the output of the schmitt-trigger inverter 4Nd to be a logic high. The output of 4Nd is then inverted by IC 5Nd. The output signals from 5Nd and 4Nf are then NORed together by NOR gate 5Nb.

When the STROBE EN signal is logic high, and the STROBE(not) signal is pulsed to a logic low, the output of NOR gate 5Nb will go to a logic high for the duration of the logic low state of the STROBE(not) signal. This transition will clock the Q output, the PR4 line, of flip-flop 5Lb to a logic low.

The PR4 line is connected to one input, pin 13, of NAND gate 5Md. A logic low on the PR4 line will act as an inhibit control to the

input circuitry for the A Relay panel, and prevent the inputting of data from the A Relay panel until the CPU has serviced the B Relay panel's keyboard input.

When the Q output of flip-flop 5Lb goes to a logic low, its Q(not) output will go to a logic high.

If the A Relay panel's keyboard is not currently being serviced, flip-flop 5Ka will be set on the next positive transistion of the system clock BF1. When flip-flop 5Ka is set, its Q output, the R4 line, will go to a logic high, and its Q(not), the S1 line, will got to a logic low.

The R4 line acts as the data buffer enable for the A Relay panel, and the S1 line acts as the data buffer enable for the B Relay panel. A logic high on the R4 line will disable the A Relay panel's data buffer 5Ja. The logic low on the S1 line will enable the B Relay panel's data buffer, 5Jb. Data buffer 5Jb will then drive the B Relay panel's data DI0(not)-DI3(not) onto the R0-R3 lines of the internal data bus.

The S1 line is connected to one input, pin 10, of NAND gate 5Mc. When S1 goes low the DRDY, data ready, line will go to a logic high. If the system is not in a RESET mode, this positive transistion of DRDY will clock flip-flop 5Ba, setting its Q output to a logic high. On the next positive transistion of the system clock, BF1, the Q output of flip-flop 5Bb will be clocked high, causing the interrupt request, BIRQ, line to go high.

The BIRQ line drives the base of transistor Q6 through resistor R4. When the BIRQ line is high, Q6 is turned ON and will place a logic low on the system's (not)IRQ line.

The positive transition of the BIRQ line will latch the keyboard input data into the tri-state register IC 5H. S1 is also latched into 5H to indicate to the CPU which Relay panel is being serviced. In addition, two inputs to 5H are supplied by switch S3, sections C2 and C3. These inputs select the ISA configuration code for the Alarm Relay Driver board.

NOTE

To ensure that the ISA configuration code, selected by switches S3C2 and S3C3, is properly read by the CPU upon power up, both flip-flops 5Ba and 5Bb are preset during the system reset

cycle. To accomplish this, the preset inputs of both flip-flops are connected to the (not)BRESET line, which goes to a logic low during all reset cycles. This will cause the BIRQ line to be set to a logic high following any system reset. Thus the ISA code will be latched into the input data register, IC 5H, so that the CPU can read it, following power up.

When the CPU responds to the IRQ and reads the Alarm Relay Driver board's keyboard data input, the address of the board's keyboard input will be decoded by the decoding section (refer to DECODING CIRCUITS).

When the keyboard input is addressed, the Y0 output of IC 3C will go to a logic low. This signal is inverted by inverter IC 5Da. The output of 5Da is NANDed with the BR/(not)W and BF1 signals by NAND gate 4Fb.

The output of 4Fb is the RDKY(not), Read Keyboard, line. The RDKY(not) line will be clocked to a logic low in sync with the BR/(not)W and BF1 signals.

A logic low on the RDKY(not) line will enable the tri-state outputs of the input data register, IC 5H, onto the data bus.

The keyboard input data R0-R3 will be driven onto bits BD0-BD3 of the data bus.

The Relay panel select line S1 is driven onto data bit BD4 of the data bus.

The ISA configuration code is driven onto data bits BD5 and BD6 of the data bus.

The RDKY(not) line will also enable the output of the tri-state buffer gate 5Af, which will drive the BIRQ line onto data bit BD7 of the data bus.

The RDKY(not) signal is inverted by IC 5Nc to form the RDKY line. The RDKY line is NANDed with the R4 line by NAND gate 5Mb. The output of 5Mb will go low when both RDKY and R4 are logic high. A logic low on the output of 5Mb will preset the B input strobe flip-flop, 5Lb.

On the next positive transition of the system clock BF1, the second flip-flop, 5Ka, will be reset. This action will result in the removal of the DRDY signal. RDKY will also clear flip-flop 5Ba.

Flip-flop 5Bb will reset on the next positive transistion of the system clock BF1. This will cause the BIRQ line to return to a logic low, causing transistor Q6 to turn OFF, allowing the system's (not)IRQ line to return to a logic high.

In the case where the A Relay panel is inputting data and the B Relay panel is not, the same sequence of events takes place except that when the A input strobe flip-flop 5La is set, its Q output will go low and act as a clear input to flip-flop 5Ka.

With flip-flop 5Ka cleared, its Q(not) output, the S1 line, will be a logic high, and its Q output, the R4 line, will be a logic low.

A logic high on the S1 line will disable the B Relay panel's data buffer 5Jb.

A logic low on the R4 line will enable the A Relay panel's data buffer 5Ja.

Data buffer 5Ja will then drive the A Relay panel's data DI0(not)-DI3(not) onto the R0-R3 data lines of the internal data bus.

Flip-flop 5Kb will be set on the next positive transistion of the system clock BF1. This will cause the Q(not) output, the S0 line, of flip-flop 5Kb to go to a logic low.

The S0 line is connected to one input, pin 9, of NAND gate 5Mc. When the S0 line goes to a logic low, the output of NAND gate 5Mc, the DRDY line, will go to a logic high.

When the CPU services the IRQ and reads the keyboard input data, as previously described, the RDKY signal generated is NANDed with S1, by NAND gate 5Ma, to preset flip-flop 5La.

On the next positive transistion of the system clock BF1, flip-flop 5Kb will be reset, and S0 will go high, resulting in the removal of the DRDY signal.

2.5.2 Alarm Relay Panel, General

Assembly: 231-4370-xx
Schematic: 231-6370-xx

The Alarm Relay panel is a remote peripheral device for use with the Alarm Relay Driver board. The panel contains 16 relays and their associated relay driver circuitry. In addition, the panel has the necessary circuitry to encode up to 20 keys.

The Alarm Relay Panel is driven by the Alarm Relay Driver board located in the mainframe. Up to two Alarm Relay Panels can be supported by an Alarm Relay Driver board.

The Relay panel contains its own power supply, which powers both the Relay panel and the interface opto-isolators located on the driving Alarm Relay Driver board.

The Alarm Relay Panel can be broken down into three main sections:

1. RELAYS AND RELAY DRIVER CIRCUITS
2. KEYBOARD ENCODER
3. POWER SUPPLY

2.5.2.1 Relays and Relay Driver Circuits

Each of the 16 relays (K0-K15) on the Alarm Relay Panel have their own relay driver circuitry. The relay driver circuitry is driven, in turn, by the output of an opto-isolator located on the Alarm Relay Driver board. There is one opto-isolator for each relay.

The driving signals, RY0(not)-RY15(not), are interfaced to the Alarm Relay Panel via connector J1. The driving signal for a particular relay is first conditioned by an RC filter network to prevent any noise picked up by the interconnecting cable from affecting the operation of the Alarm Relay Panel.

The output of the conditioning circuit is applied as the input to a 74C14 CMOS schmitt-trigger inverter (Z12, Z14, and Z16). The output of the schmitt-trigger is used to drive the relay driver made up from one section of a ULN2003A (Z13, Z15, and Z17). The output of the ULN2003A drives the relay (K0 - K15). The relay coil is shunted by a 1N914 diode to protect the driver from the current spike generated when the relay coil is de-energized.

Each relay has both normally open (NO) and normally closed (NC) contacts. The common of each relay is connected to the appropriate position on terminal strip TB5. The "NO" contact of each relay is connected to the appropriate position on terminal strip TB6. The "NC" contact of each relay is connected to the appropriate position on terminal strip TB4.

2.5.2.2 Keyboard Encoder

The Alarm Relay Panel has the necessary circuitry to encode 20 keys. However, only the first 16 keys are used. The keys may be any form of SPST momentary switch that is normally open. The encoded data is sent via connector J1 to the Alarm Relay Driver board located in the mainframe.

IC Z1 is a free-running oscillator which acts as the master clock source for the encoder circuitry. The output of Z1 is connected to the two NAND gates Z2a and Z2b. NAND gate Z2a is wired as an inverter. Its output drives the CLK line, which is the master clock line for the encoder circuitry. The second input to NAND gate Z2b is the (not)LATCH signal which, is generated by the encoder logic. The output of Z2b is the GCLK, Gated Clock, line which acts as the clock for the scan counter, IC Z7.

The scan counter, Z7, is an 8-stage binary counter of which only the first six stages are actively used. The counter is clocked by the negative transistion of the GCLK line. The SC output of Z7 is inverted by inverter Z8c to form (not)SC. The outputs, DA through DE, and SC, from Z7 along with (not)SC, are applied to the three 1-of-8 decoders (Z3, Z4, and Z5).

The outputs of the decoders form 20 discrete logic low going key strobe signals. Only one key strobe signal is logic low at a time. The eight outputs of Z5, and the lower two outputs of Z3, form the S0-S9 lines that are sent to terminal strip TB0. The upper six outputs of Z3, and the lower four outputs of Z4, form the 10-19 lines that are sent to terminal strip TB2.

Each terminal on TB0 can be wired to one side of a momentary, normally open, SPST switch. The other side of the switch is then wired to the appropriate terminal on terminal strip TB1. The same is true for TB2 and TB3.

When a switch is closed, scan counter Z7 is clocked to the point at which the corresponding decoded key strobe goes to a logic low.

At that time, the input diode in the opto-isolator, IC Z9, will turn ON. Its ON current will be sunk to ground through the closed switch and the output driver in the corresponding decoder. The output of the opto-isolator will go to a logic low. The output of the opto-isolator is inverted by inverter Z16f. Z16f is a 74C14 schmitt-trigger inverter which helps to ensure a clean response to a switch closure.

When the output of the opto-isolator goes to a logic low, the output of inverter Z16f will go to a logic high. The output of Z16f is connected to the 4D input, pin 13, of the quad flip-flop, IC Z6. On the next positive transition of the CLK line, the fourth stage of Z6 will be set. The Q4(not) output, pin 14, of Z6 will go low, and cause the output of NAND gate Z2d, which drives the LATCH line, to go to a logic high.

The LATCH line is connected to the clock input of the output data register, IC Z11. The positive transition of the LATCH line will latch the current output lines, DA-DE, of the scan counter, Z7, into the output data register, Z11. The outputs of Z11 drive inverters Z8a, Z8b, Z8d, Z8e, and Z8f, which act as buffers to drive the data onto the cable that connects the Alarm Relay Panel to the Alarm Relay Driver board located in the mainframe.

The latched and buffered DA-DD lines become the DI0(not)-DI3(not) lines, that are sent to the Alarm Relay Driver board in the mainframe. The latched and buffered DE line becomes the STROBE EN line which is sent to the Alarm Relay Driver board. The LATCH line is inverted by inverter Z10f to drive the (not)LATCH line, which is used as the gating control by NAND gate Z2b in generating the GCLK line. This will cause the GCLK line to remain in the logic high state, and thus stop the scan counter, Z7.

The LATCH line is also connected to the 1D input, pin 4, of the quad flip-flop Z6, and to one input, pin 10, of NAND gate Z2c. The Q4 output, pin 15 of Z6, is connected to the 3D input, pin 12, of Z6.

On the next positive transition of the CLK line, the first and third stages of Z6 will be set. The Q1 output, pin 2 of Z6, will go to a logic high, and the Q3(not) output, pin 11 of Z6, will go to a logic low. The Q1 output of Z6, pin 2, is the second input to NAND gate Z2c. When Q1 goes to a logic high, the output of Z2c will go to a logic low. This signal is connected to the 2D input of the quad flip-flop Z6.

On the next positive transition of the CLK line, the second stage of Z6 will be reset and the Q2(not) output, pin 6 of Z6, will go to a logic high. The Q2(not) output of Z6 is inverted by inverter Z10a. Inverter Z10a acts as a buffer to drive the data STROBE(not) signal onto the external cable that connects the Alarm Relay Panel to the Alarm Relay Driver board in the mainframe.

When the switch is opened, the input diode of the opto-isolator Z9 will turn OFF, and its output will go to a logic high, pulled up to +5 volts by resistor R7. This will cause the output of Z16f and thus the 4D input to Z6 to be low.

On the next positive transition of the CLK line the fourth stage of Z6 will be reset. This will cause the Q4 output to go to a logic low, and the Q4(not) output to go to a logic high. With the Q4 output logic low, the 3D input is also logic low.

On the next positive transition of the CLK line, the third stage of Z6 will be reset, and it's Q3(not) output will go to a logic high. When both Q3(not) and Q4(bar) are logic high, the output of NAND gate Z2d, the LATCH line, will go to a logic low that will enable the GCLK line through the operation of NAND gate Z2b. The logic low on the LATCH line will also cause the output of Z2c to go to a logic high and thus the 2D input of Z6 will be a logic high.

On the next positive transition of the CLK line, the second stage of Z6 will be set, and the Q2(not) output of Z6 will go to a logic high. This will cause the output of inverter Z10a to go to a logic low, and thus remove the STROBE(not) signal going to the Alarm Relay Driver board in the mainframe. Also, the first stage of Z6 will be reset, causing the Q1 output to go to a logic low.

The keyboard encoder circuitry is now ready to service the next switch closure.

2.5.2.3 Power Supply

The power supply provides +24 volts for the relays and +5 volts for the digital logic devices on the Alarm Relay Panel. In addition, the +5 volts produced on the Alarm Relay Panel is also sent, via connector J1, to the Alarm Relay Driver board, to power the keyboard input data opto-isolators.

The power supply consists of transformer T1, rectifiers CR18

through CR21, filter capacitor C23, and regulator Z18.

The output of the secondary winding of T1 is applied to the full-wave bridge rectifier, CR18 through CR21. The DC voltage from the bridge rectifier is filtered by capacitor C23 and is approximately 24 volts. The filtered 24 volts is used to power the relay coils.

The filtered 24 volts is also applied to the input of regulator IC Z18. The output of Z18 is a regulated +5 volt, used to power the digital devices on the Alarm Relay Panel, and the opto-isolators located on the Alarm Relay Driver board. Regulator Z18 is mounted on a heat sink to help dissipate the heat produced by the device.

As an alternate power source, a 24 volt battery may be connected to the Alarm Relay Panel by connecting the battery terminals to TB7. A diode is be used to isolate the battery from the main power supply.

2.5.3 Digital Inputs Board, General

Assembly: 231-4350-xx
Schematic: 231-6350-xx

The Digital/Status board is designed to operate in one of three different user selectable modes: digital input mode, status mode, and events mode.

In the "Digital Input" mode, it enables reading data into the mainframe from an instrument equipped with a digital output feature. In this mode it provides a full handshake via the READY and BUSY lines for each eight bits of digital data.

In the "Status" mode, it can be used to read in the status of active or passive circuitry. Six isolated five volt power supplies are provided to support the passive devices.

In the "Events" mode, a change of state on any one of the 48 input lines will cause an interrupt to be generated, signaling the mainframe software that an event has taken place.

The Digital/Status board can be functionally divided into the following sections:

1. INPUT FILTER
2. I/O ISOLATOR
3. LOGIC LEVEL CONTROL
4. PERIPHERAL INTERFACE
5. EVENTS TRIGGER DECODER
6. TIMING AND ADDRESS DECODERS
7. BUS BUFFERS
8. ISOLATED AUXILIARY POWER SUPPLIES

2.5.3.1 Input Filter

All external inputs to the Digital/Status board pass through RC filters where high frequency noise is removed. Each filter consists of a 2.2Kohm resister in series with the input signal, followed by a .01 microfarad capacitor connected to that signal's ground.

Resistor networks RN7 through RN12, along with R1, R5, R9, R13 R17 and R21, provide the necessary 2.2Kohm resistors, while capacitor networks CN1 through CN6, along with C2, C4, C8, C8, C10 and C12, provide the .01 microfarad capacitors.

2.5.3.2 I/O Isolators

Each external signal coming onto, or off of, the Digital/Status board is isolated from the mainframe's digital power supply by the ILCT6 opto-isolators, Z33 through Z62.

All inputs are required to provide a sink current of 1.6 milliamperes in the low state, and no current in the high state. Corresponding voltages are 1.5 volts or lower for a low, and 4 volts or higher (up to 15 volts) for a high. Surge protection on each opto-isolator is provided by diodes CR7 through CR60.

Each BUSY output will drive one TTL load (1.6 milliamps) through transistors Q1 through Q6. These outputs are protected against overvoltage by the 5.6 volt zener diodes, CR1 through CR6.

2.5.3.3 Logic Level Control

Positive or negative logic levels are switch selectable for all of the external signals to and from the Digital/Status board. Each input signal is brought into one input of a CMOS exclusive OR

buffer, 74C86. The second input to these buffers comes from the DIP switch, S2. Switch S2-7 selects the logic level of the READY input, while S2-8 selects the logic levels of the 48 digital inputs. With S2-7 in the OFF position, the 6.8Kohm pull up resister, R36, holds the second input to the six "READY" exclusive OR buffers at 5 volts. This causes the READY signals to be inverted before being passed on to the peripheral interface. Likewise, switch S2-8 in the OFF position allows the 6.8Kohm pull up resister, R31, to hold the second input of the "digital" exclusive OR buffers at 5 volts. This will invert all 48 incoming digital signals. With switch S2-7 or S2-8 in the ON position, the second input to the "READY" or "digital" exclusive OR buffers is held at ground. This allows the incoming signals to pass on to the peripheral interface section unchanged.

Switch S2-6 controls the logic level of the BUSY output. With this switch in the OFF position, the 6.8Kohm pull up resister, R35, holds the second input of the "BUSY" exclusive OR buffers at 5 volts. This will invert all six BUSY outputs before they leave the board. With switch S2-6 in the ON position, the second input to the "BUSY" exclusive OR buffers is held at ground. This allows the BUSY signals to leave the board unchanged.

2.5.3.4 Peripheral Interface

The peripheral interface section consists of the three PIAs (Peripheral Interface Adapters) Z7, Z8 and Z9, and is the actual interface between the peripheral world and the microprocessor bus.

The three PIAs are configured as input devices, during the power on initialization sequence, by storing all zeroes into their data direction registers. The control registers are then initialized, and the settings of the MODE SELECT switch (S2-1, S2-2 and S2-5) are determined by reading the CB2 status flag in each PIAs control B register. Any further programming of the PIA is then done by the software.

Each PIA acts as two, 8-bit wide gates. Data present on the input to the PIA is gated onto the microprocessor's data bus whenever the processor performs a READ operation from the memory location assigned to one of the PIA peripheral data registers.

The PIA interrupt inputs, CA1 and CB1, on all three PIAs, are used as the handshake input (READY) in the BCD mode, while the handshake output (BUSY) is controlled by CA2 and CB2. Since no

handshaking occurs in the "Status" or "Events" modes, CB1 on Z9 is used as the EVENTS TRIGGER input in the "Events" mode.

2.5.3.5 Events Trigger Decoder

The 48 digital input signals are also connected to six 74C30, eight input NAND gates (Z10 through Z12 and Z15 through Z17). In the "Events" mode, all inputs are required to be in the same state (open or closed) initially. Switch S2-8 is used to ensure a high level at the input to the NAND gates.

When there is a change of state (event), one or more of the NAND gate inputs will go to ground. This will cause one or more of the NAND gates to output a high instead of its initial low. All of the NAND gate outputs are inverted by the 74C04 hex inverter, Z14. These are then fed into six inputs of another 74C30 eight input NAND gate. The remaining two inputs are tied directly to 5 volts. The output of this NAND gate is tied, via switch S2-3, to the CB1 input of PIA Z9. Thus, when an event occurs, this line will immediately go high, causing the CB1 status flag in the control B register of PIA Z9 to be set.

2.5.3.6 Timing and Address Decoders

A mainframe may contain up to two Digital/Status boards, each responding to unique addresses within the microprocessor's memory space. Address bits A15 through A9 are the same for both board No.1 and board No.2.

These address lines are decoded by the 74LS27 three input NOR gates, Z3, and the 74LS10 three input NAND gates, Z5. The VMA line is connected to a 74LS04 hex inverter Z6, and is also used in the decoding. When a valid PIA address is asserted on the bus, the appropriate decoding takes place, and a Valid Board Address (VBA) signal, and a Data Bus F1 Enable (DBFE) signal, goes high.

Address bits A8 through A5 are used to select the individual Digital/Status boards. These four lines are connected to the 74LS42 four-to-ten line decoder, Z2. Outputs one through six are connected to DIP switch S1.

With switches S1-1, S1-2 and S1-3 in the ON position, the board will respond to hex addresses 242X, 244X and 246X. With switches

S1-4, S1-5 and S1-6 in the ON position, the board responds to hex addresses 248X, 24AX and 24CX. Outputs seven through nine are connected to DIP switch S3. This switch is only installed on certain maintenance test boards, and causes the board to respond to hex addresses 24EX, 250X and 252X. Each of the three switch selected outputs is connected to one of the chip select inputs on PIA Z7, Z8 or Z9.

The microprocessor clock is buffered by the 74LS04 hex buffers, Z6, producing two timing signals, IT and OB. The OB signal is connected to the enable (E) input of each PIA, while IT is connected to switch S2-1, S2-2 and S2-5, where it is used during the board initialization process.

2.5.3.7 Bus Buffers

The Digital/Status Board interfaces to the mainframe by means of the mainframe bus, which is buffered by the 74LS245 octal bus transceiver, Z1. Read/write, reset and IRQ are buffered by the 74LS244 octal buffer, Z4, as are address lines A0 and A1. This board adds one 74LS load to the mainframe bus. All timing signals are in accordance with the mainframe bus timing specification.

2.5.3.8 Isolated Auxiliary Power Supplies

Six isolated, auxiliary power supplies are provided to support devices which operate in a passive mode. Phases 1 and 2 of the mainframe power supply drive the primary winding of transformers T1 and T2. Phases 1 and 2 are 15 KHz square-waves of opposite phase, with a voltage swing of approximately 12 volts (-6v to +6v).

The output of each transformer is half-wave rectified and filtered by diodes CR67 through CR72 and the 22 microfarad tantalum capacitors C13 through C18. Each secondary winding, along with its associated circuitry, provides one isolated supply of 5.5 volts (+/- 10%) at 20 milliamperes. Over voltage protection is provided on each power supply by the 6.8 volt zener diodes CR61 through CR66.

3 Troubleshooting

3.1 INTRODUCTION

In this section of the manual, we will discuss board level type troubleshooting procedures for the Digitrend 245 data logger system.

The procedures are based on a systematic process of elimination as determined by the symptoms. This approach--which narrows down the possibilities until the faulty board is found--will allow you to quickly determine which board (or boards) failed without the need for elaborate test facilities.

Only the main system boards in the mainframe unit (refer to 2.2) will be covered in detail in sub-section 3.3 and related paragraphs. A short discussion of satellite troubleshooting is found in 3.4.

3.2 PRELIMINARY TROUBLESHOOTING

Before attempting to troubleshoot the instrument, first make sure that the difficulty is actually due to a malfunction within the instrument and not due to improper control settings, signal connections, or power source problems. This is done by (a) inspecting the ac line cord connections and making sure that the ac socket being used is active, (b) checking the condition of the ac fuse, (c) making sure the mainframe keyswitch is ON, (d) inspecting all input signal connections, (e) checking any satellite interconnecting cables, and (f) re-programming the unit to ensure that no programming error exists.

3.3 SYSTEM SUPPORT TREE

When external causes are ruled out, you have two primary approaches to locating the faulty circuit board. You can either perform a board by board substitution (if substitute boards are available) until the problem is resolved, or follow the procedures set forth in this section to isolate the failure to a particular board. The latter method will allow the you to isolate the failure without requiring a complete set of spare boards.

The Digitrend 245 data logger system is based on a microprocessor and contains all the basic elements of a full computer system. The interaction of each board within the system and the microprocessor can result in a variety of symptoms in the event one of the boards fail.

Before you can isolate the problem down to a particular board, you must first have some understanding of the dependency of the various boards within the system upon each other. For that reason, the troubleshooting procedures set forth in this section are based upon a system support tree.

In order to ease the troubleshooting task, think of the instrument as a stack of boards, or blocks. The position of each block in the stack is dictated by the function of the block and the way in which it relates to the other blocks. The man/machine interface items (displays, keyboard, printer, and audible beeper) form the blocks which reside at the top of the stack, while the power supply resides at the bottom of the stack.

Due to this relative structure, if any of the blocks below the audio-visual blocks fail, the audio-visual blocks will generally provide some form of abnormal operation which will not only alert you to the system failure but can also supply clues that can help you in determining the source of the failure.

The chart below shows the relative block level of the board assemblies in the mainframe:

LEVEL	ASSEMBLY
4	FRONT PANEL BOARD
3	PERIPHERAL INTERFACE ADAPTER (PIA) BOARD
3	OPTION BOARDS
3	FEMs
2	CENTRAL PROCESSOR UNIT (CPU) BOARD
1	MAIN BOARD
0	POWER SUPPLY MODULE

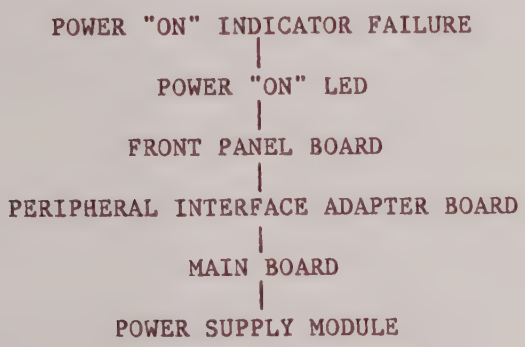
Based on the symptoms present and the relative order of dependency of the system blocks, courses of action are prescribed to isolate the cause of failure. As an example of this dependency, all system blocks are dependent upon the power supply module and thus are supported by it. All system blocks, except the power supply module, are dependent upon the central processor board and thus

are supported by it while the central processor board is supported by the power supply module. (Sort of the electronic equivalent of "the hip bone is connected to the leg bone...")

3.3.1 Power Supply Troubleshooting

SYMPTOMS: no power ON indicator, no display, and/or no printer activity.

Shown below is a typical failure support tree for the power supply module:



The power supply accepts the ac line voltage and produces the various regulated voltages required by the data logger's circuits. The voltages produced are +5 volts, +12 volts, and -12 volts along with two square wave power outputs (15 kHz, phase1 and phase2) which are used for FEM operation.

All troubleshooting should begin by observing the POWER ON LED indicator on the front panel to tentatively verify that the power supply module is operational. If the POWER indicator does not turn on when the keyswitch is in either the "ON" or "PRGM" position. then the failure is linked to the power supply module or to the Front Panel board.

Measure the voltage of the +5 volt supply on the main board. The measurement can be made on the power supply bus of the main board between pin 1 (GND) and pin 2 (+5V). The voltage read should be between +4.75 and +5.5 volts. If the voltage read is within this range, the failure is either on the PIA board or on the Front Panel board.

If the supply voltage measured was not in the above range, try adjusting the voltage with the +5V adjust on the power supply module. If the supply can be adjusted to fall within the proper range, then re-evaluate the symptoms.

If the power supply can not be adjusted to a level within the proper range, or if there is no voltage output from the supply, it is probably the source of the failure. You should then check out the power supply.

****
* WARNING *
****

Hazardous voltages exist in and around the power supply circuitry. Use extreme caution when testing voltages and connections on the power supply board.

First remove the power cord from the power supply. Next remove the line fuse and check to see if it is still good. If the fuse is blown, replace it. With the power cord removed and the keyswitch in the "OFF" position, remove the power supply grounding lug and remove the power supply from the card cage. Place the power supply board on a non-conducting surface and reconnect the power cord. Leave the interconnecting cable between the power supply and the front panel connected.

Turn the front panel power switch to the "ON" position. Measure the voltage between pin 23 (+5V) and pin 28 (GND). If the measured voltage is not within the allowable voltage range of +4.75 to +5.25 volts, adjust potentiometer R7 for a value within this range. (Refer to the power supply assembly drawing for the location of this pot.) If R7 cannot be adjusted within the range, the supply is defective and must be repaired or replaced.

If the +5 volt supply output reads normally, then check the +12 and -12 volt supply outputs (refer to the power supply module schematic diagram 231-6500-xx for the proper pin numbers). If the supply operates normally when out of the card cage, but does not operate when plugged in, there are two possible causes:

1. There is a short on one of the power busses.

2. The supply has been damaged and cannot supply the current levels required.

If an ohm meter is available, use it to check for a shorts between the power busses and the ground busses. If a short is found, remove all circuit board assemblies within the unit, one board at a time until the short is removed. If the short is still present after removing the last board, the short is somewhere on the main board. The main board should then be repaired or replaced.

If the ohm meter check is inconclusive, plug the supply back into the card cage (first make sure that the data logger is turned OFF). Now, turn the unit ON and check the power supply output voltages from the main board test connector (J11, which is on main board behind front panel) as you remove each board/module from the unit one at a time. If a supply line goes back to a normal level after a board/module is removed, then that board/module is the one causing the abnormal load.

CAUTION

To avoid possible damage, do not insert a board/module in the card cage with power ON.

If the short or abnormal load is still present with all the boards removed, then the main board should be checked for any shorts. If the main board is OK, then the power supply itself is defective, and should be repaired or replaced.

3.3.2 CPU Board Troubleshooting

The CPU board is the functional center of the mainframe unit, all the other boards in the mainframe, except the power supply, are dependent upon it. If the data logger resets for unknown reasons, fails to run for even a limited period of time, or fails to run at all, the CPU board should be checked.

To determine if the problem is in the CPU board, first make sure that the mainframe keyswitch is in the "OFF" position. Then remove all FEMs and option boards (if any) from the card cage. In this stripped down form, turn the power ON and check to see if the data logger is operational. If the data logger still fails to operate, the problem is likely to be on the CPU board. Swap the suspect CPU board with a known good one to determine if it is indeed defective.

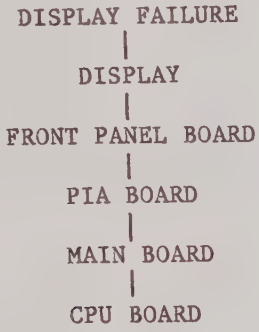
3.3.3 PIA Board/Front Panel board Troubleshooting

The PIA board forms the major interface link between the central processor (CPU), and the Front Panel board and FEMs. Through its interaction with the Front Panel board, it supports all of the man/machine interfaces, the displays, keyboard, printer, and beeper. The PIA board also acts as the interface through which all communication between the central processor and the FEMs takes place. The PIA board also supports the watchdog circuitry which monitors operation of the mainframe unit.

A failure in the PIA board can result in a failure appearing in the display, the keyboard, the beeper, the printer, the FEMs, or the watchdog system.

3.3.1.1 Display

Shown below is a typical failure support tree for the display:



Turn the mainframe keyswitch to the "ON" position and press the "PAPER" key. All segments of each digit should light. If an individual digit or an individual segment within an individual digit fails to light, the problem is on the Front Panel board. This board should then be repaired or replaced. If all numeric displays have the same segment failure, short pin 7 of IC 2A on the Front Panel board to the appropriate pin on IC 2H on the PIA board as shown in the following table:

IC 2H PIN	SEGMENT
1	a
2	b
3	c
4	d
5	e
6	f
7	g
8	dec. pt.

If the segment in question fails to light during this test, the Front Panel board should be repaired or replaced. If the segment does light during this test, the PIA board should be repaired or replaced. If the segment did not light during this test, and replacement of the Front Panel board did not correct the problem, the interconnecting cable between the PIA board and the front panel board should be replaced. If this action does not correct the problem, the cause of failure may be on the CPU board.

If, when pressing the "PAPER" key, only one display is lit, and paper does not advance, the Front Panel board, interconnecting cable, and the PIA board should be replaced in that order until normal display operation is restored. If normal display operation is not restored after replacement of these items, the CPU board and power supply should then be checked for proper operation.

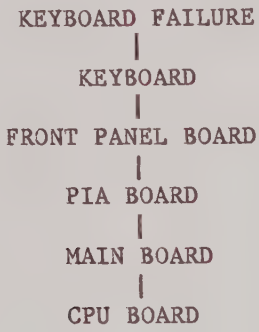
If all displays light and paper advances when the "PAPER" key is pressed, then press the "CLEAR" key and observe that all numeric displays are extinguished. If any display or individual segment of a display remains lit, there is a problem with the Front Panel board and it should be replaced. If replacement of the Front Panel board fails to correct the problem, then the CPU board should be checked.

If the display responds correctly to the above tests, but is dim in appearance, the +5VL supply from the power supply should be checked. If the +5VL supply is below +5 volts, the power supply should be checked or replaced. If the +5VL supply is at +5 volts then verify that, when the data logger is displaying the time, the seconds digits of the clock display advance at a 1 Hz rate. If the clock operates normally, then the Front Panel board and the interconnecting cable should be checked and replaced as required. If the clock fails to operate normally, first the PIA board, and then the power supply should be checked and replaced if required.

If no problems are found with the PIA board or the power supply, the CPU board should be checked.

3.3.1.2 Keyboard

Shown below is a typical failure support tree for the keyboard:



In order to properly diagnose a failure on the keyboard, it will be necessary to first press the "CLEAR" key followed by one of the other keys on the keyboard. The display should respond accordingly to the key being pressed (i.e. pressing "PRGM" results in "P" being displayed). This sequence is repeated for each key on the keyboard. The sequence should be performed in rows of keys on the keyboard. It should be noted which key(s) if any are not functioning when this test sequence is performed.

If an entire row of keys are inoperable, the problem can exist on the Front Panel board, the PIA board, or the keyboard itself. To test for the source of the failure, a jumper should be placed across the appropriate pins of IC 2A (a 4010) on the front panel board per the table below, and the function of that row re-tested. Shown below is the jumper connections required for testing each row:

JUMPER CONNECTIONS FOR IC 2A

KEY	PIN	CONNECTS TO	PIN
CLEAR	3		2
PRGM	15		14
CALIB	12		11
RESET	10		9

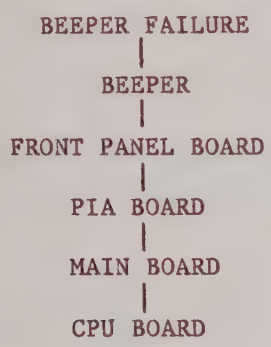
If a given row of keys is still inoperable, the problem is either on the PIA board or the keyboard itself. The PIA board should be tested and replaced if necessary before any attempt is made to replace the keyboard. If the row of keys operate normally with the jumper on IC 2A, then replace the Front Panel board.

If a given column of keys are inoperable, then the problem is on the Front Panel board and it should be replaced. If only one key is inoperable, then the problem is probably on the keyboard itself and it should be inspected and replaced if required.

If replacement of the appropriate boards, as outline above, does not correct the keyboard failure, then the failure may be in the CPU board. The CPU board should be checked and replaced if required.

3.3.1.3 Beeper

Shown below is a typical failure support tree for the beeper:

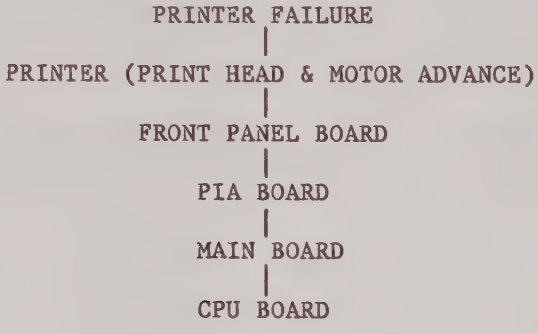


If the beeper fails to operate when a key is pressed or on power ON/OFF cycles, a failure may exist on either the Front Panel board or on the PIA board. Use a screw driver and adjust pot R44 on the Front Panel board while repeatedly pressing the "CLEAR" key. If the beeper can be adjusted to an acceptable level, the beeper is alright. If pot R44 has no effect, attach a jumper to pin 9 of IC 1E on the Front Panel board. Then alternately connect the other end of the jumper to pin 8 and pin 16 of IC 1E. If the beeper is operable it should beep. If it beeps during this test, the problem is probably on the PIA board and it should be replaced. If the beeper fails the test then the Front Panel board is the source of the problem and it should be replaced.

If a beeper problem is occuring in coincidence with a keyboard problem, correct the keyboard problem first.

3.3.1.4 Printer

Shown below is a typical failure support tree for the printer:



Problems with the mainframe's printer on can arise from four places, the printer motor, the print head, the Front Panel board, and the PIA board. The printer interconnect cable should be inspected first when the printer shows any problems in operation.

The printer normally prints 12 digits across the width of the paper with each digit being 5 segments wide and 7 segments high. If only one or two segments are out on the print head (i.e. not printing) then the print head should be replaced. If the same segment in each digit position is out, then the front panel board should be checked and replaced if required. If a single digit fails to print, then the Front Panel board and PIA board in that order should be checked and/or replaced.

3.4 SATELLITE TROUBLESHOOTING

Problem symptoms of a satellite include not getting data from a satellite, not getting data from a particular FEM in a satellite, or no communication at all with a satellite ("No Sat" error message).

Other than the FEM modules, a satellite unit has two main circuit board assemblies: the power supply and satellite controller board. This makes fault isolation of any satellite problems relatively simple.

If there appears to be no communication with a satellite ("No Sat" error message), first check that the satellite power is plugged in and that the "Power On" indicator on the front panel of the satellite is ON:

If the satellite appears to be dead when plugged in, then check the power supply module (refer to 3.3.1).

If the satellite's "Power On" indicator is ON, check the satellite/mainframe interconnection. If this checks OK, connect the suspect satellite to another satellite connector (one that you know is working) on the mainframe rear panel to see whether it's the mainframe causing the problem. If the result is the same with the alternate mainframe connector, swap the satellite controller board with a known good one. If operation is restored, the replaced controller board was defective. If operation is not restored, the power supply is not supplying the correct output voltage and should be repaired or replaced.

If you are not getting data from a particular point, first check the input sensor wiring for integrity. If this checks OK, then the FEM holding that point is likely to be at fault.

If you are not getting data from all points of a particular FEM, first check that the FEM is securely in the card cage. If this checks OK, then swap the suspect FEM with a known good one. If the problem goes away, then the replaced FEM was defective. If the problem is still there, then the satellite controller board is likely to be at fault.

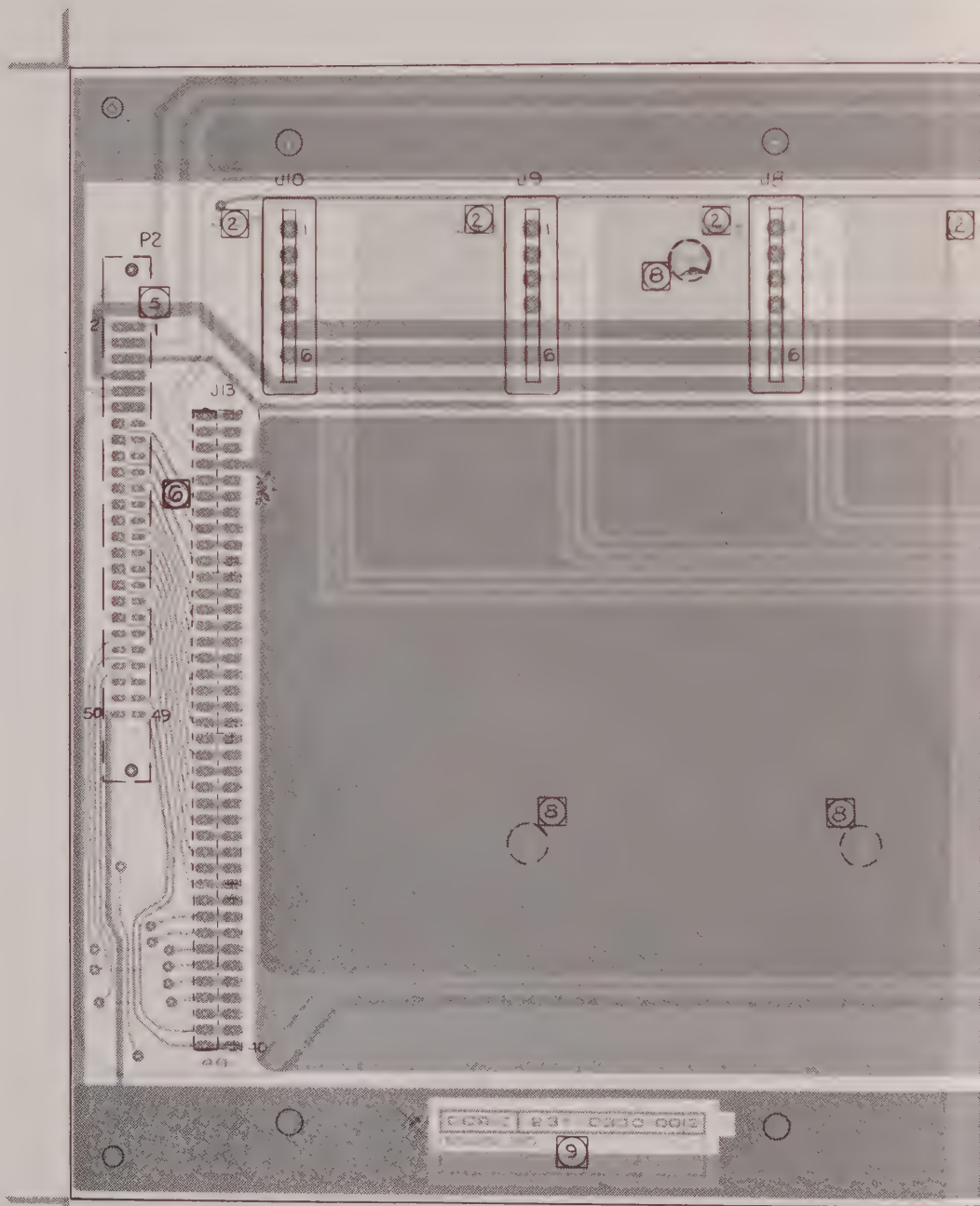
If you are not getting data from all FEMs within a satellite, but there is no communication error message ("No Sat"), the satellite's power supply to the FEMs is likely to be at fault. Check the power supply for active 15 kHz phase1 and phase2 lines with an oscilloscope. If this checks OK, then the satellite controller board is likely to be at fault.

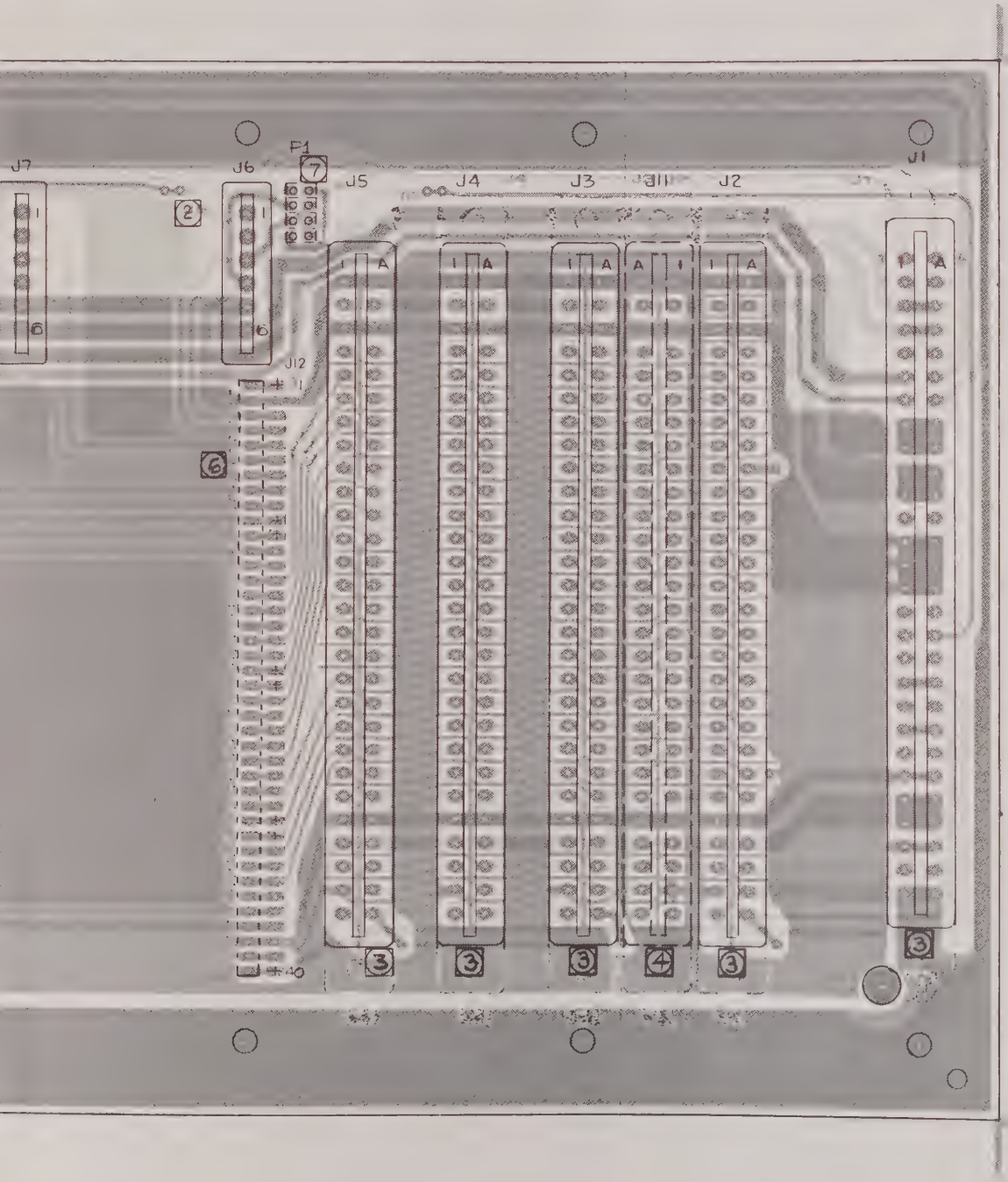
4 Drawings

4.1 INTRODUCTION

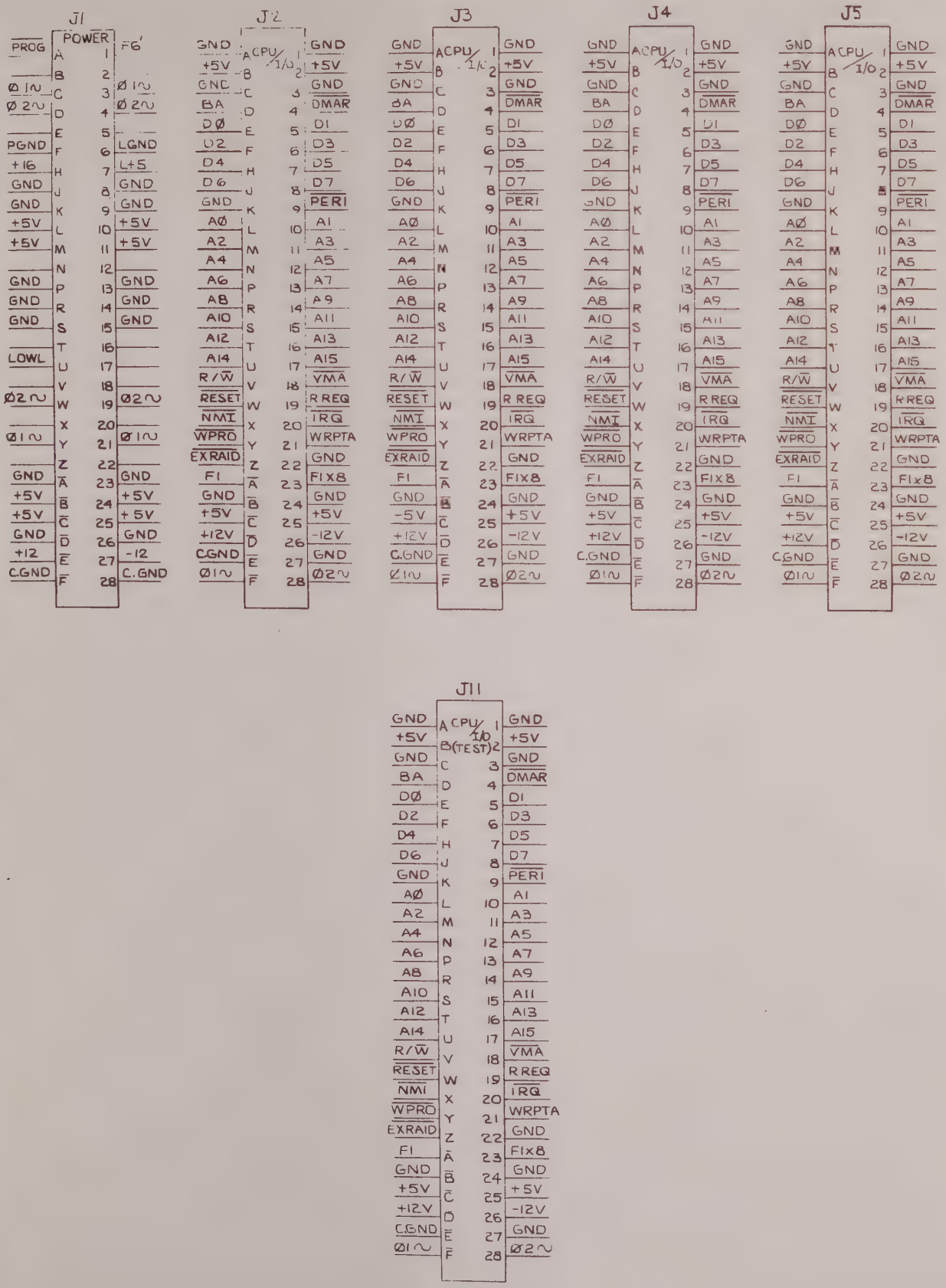
Drawings for the Digitrend 245 data logger system circuit board assemblies are given to you in this section of the manual. For each circuit board assembly, the following is given (in order): (1) PCB top assembly drawing, (2) schematic diagram, and (3) parts list. This section is divided into three basic parts:

* Mainframe boards
* FEMs and Remote FEM I/O cards
* Satellite Controller board

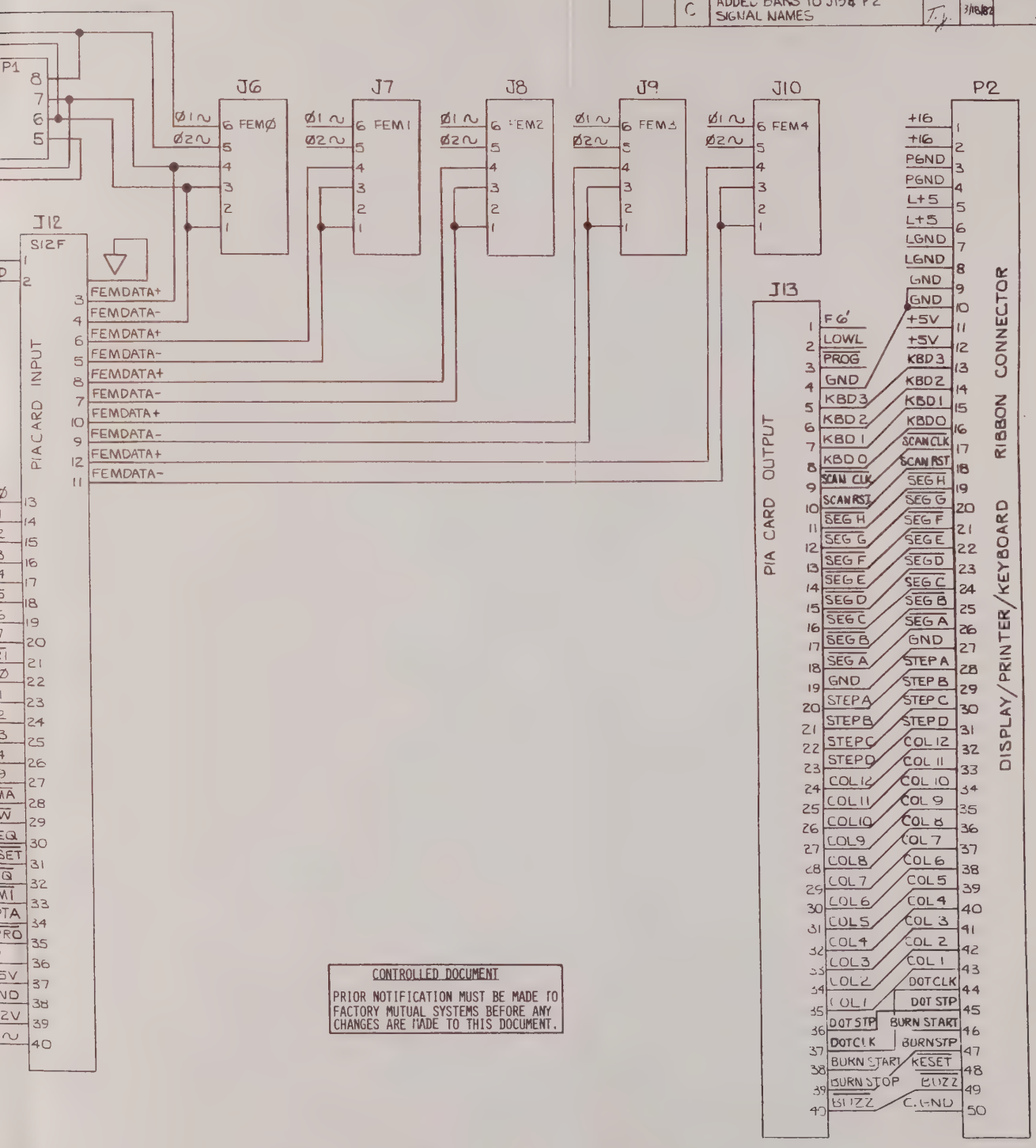

J10
J9
J8
P2
J13
50
49
1
10



ASSEMBLY
-MAIN BOARD
231-4300-00 E


J1
POWER
PROG
F6'
Ø1~
Ø2~
PGND
LGND
+16
L+5
GND
GND
GND
+5V
+5V
+5V
LOWL
Ø2~
Ø1~
GND
GND
GND
+5V
+5V
+5V
GND
GND
GND
+12
-12
C.GND
C.GND
J2
ACPU 1/O
GND
+5V
GND
BA
DØ
D2
D4
D6
GND
AØ
A2
A4
A6
A8
A10
A12
A14
R/W
RESET
NMI
WPRO
EXRAID
FI
GND
+5V
+12V
CGND
Ø1~
GND
+5V
GND
DMAR
DI
D3
D5
D7
PERI
AI
A3
A5
A7
A9
A11
A13
A15
VMA
R REQ
IRQ
WRPTA
GND
FIX8
GND
+5V
-12V
GND
Ø2~
J3
ACPU 1/O
J4
ACPU 1/O
J5
ACPU 1/O
J11
CPU 1/O
B(TEST)

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A1	[illegible] RELEASE	[illegible]	[illegible]	[illegible]
		A2	REVISED PER E.O. 2-10225	[illegible]	[illegible]	[illegible]
		B	PRODUCTION RELEASE PER E.O. 2-10403	[illegible]	[illegible]	[illegible]
		C	ADDED BARS TO J13 & P2 SIGNAL NAMES	[illegible]	3/18/82	DWS



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	DRAWN	[illegible]	[illegible]		SCALE	DO NOT SCALE DRAWING	SHEET 1 OF 1
	CHECK	[illegible]	[illegible]				
	APPR.						

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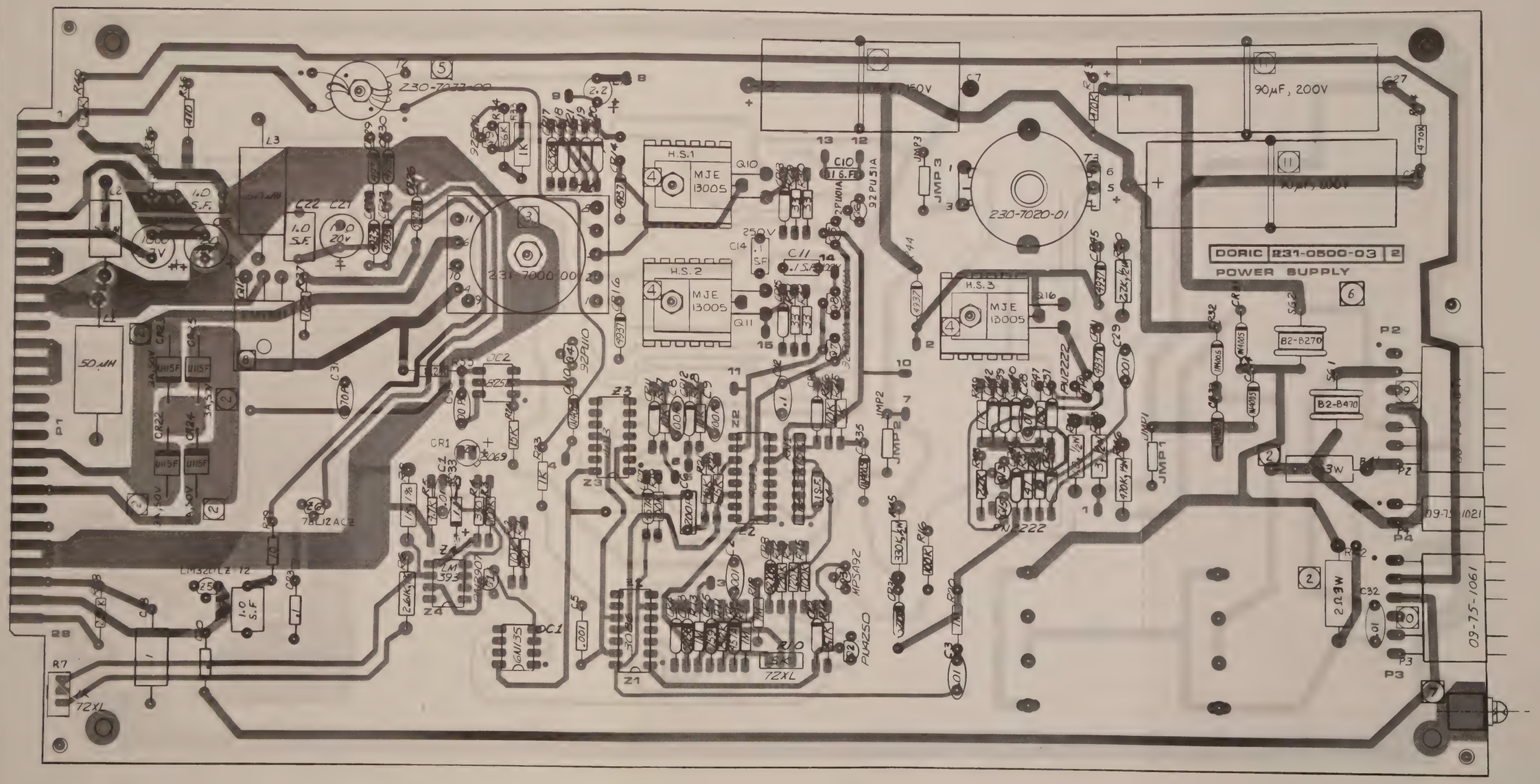
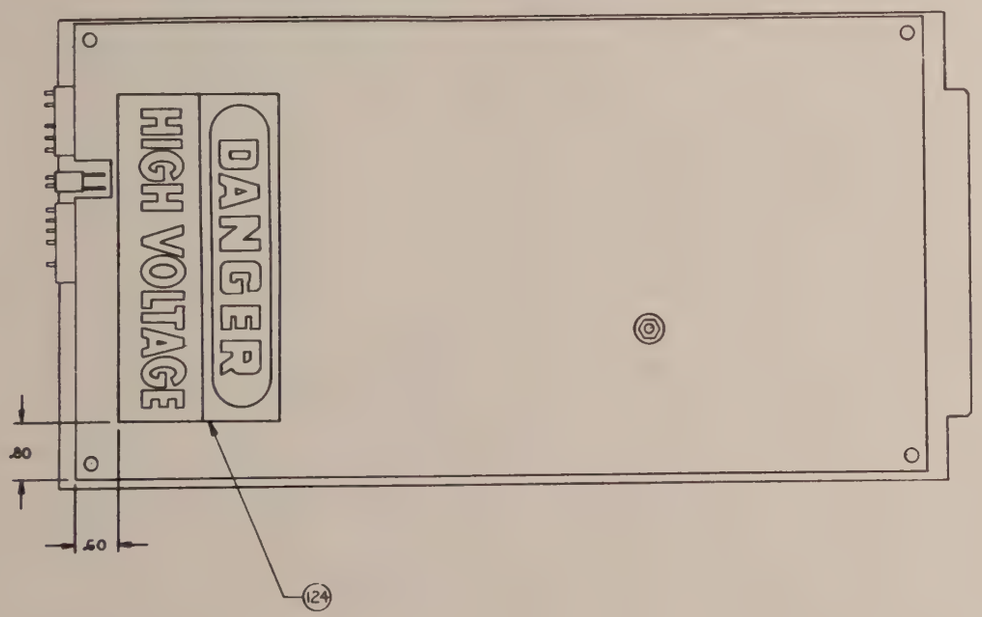
DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, MAIN BOARD	MODEL NO. 235	DATE 2-27-80	SHEET 3 OF 3

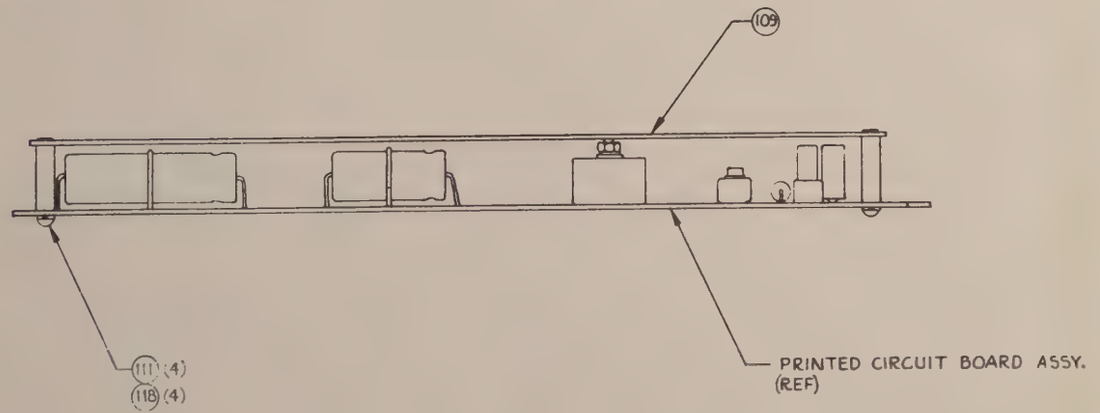
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, MAIN BOARD	231-2300-00	1	
2	SCHEMATIC	231-6300-00	1	
3	TEST SPEC		1	
4				
5				
6	CONN, PC 56 AMP. 3-53066602	973-0101-07	6	J1-J5,J11
7	CONN, PC 6 VIKING 2VH6/1AK12	973-010-51	5	J6-J10
8	CONN, PC 50 RIBBON (3M3433-2203)	973-060-10	1	P2
9	CONN, 40 P .1 CTR 1-87334-8	973-0101-21	2	J12,J13
10	TERM STICK 8M (65611-108) BERG	973-381-01	1	P1
11	STDF, 7/16 X 440A3	991-020-01	3	



ASSEMBLY -
POWER SUPPLY
231-4500-03B

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED





SIZE	CODE IDENT. NO.	DRAWING NO.	CHANGE LETTER
D		231-4500-03	B
SCALE 1	DO NOT SCALE DRAWING	SHEET 2 OF 3	

REFERENCE DESIGNATORS		
	LAST USED	DO NOT USE
RESISTORS	R55	
CAPACITORS	C33	
DIODES	CR45	
RES NETWK	RN1	
TEST POINTS	TP15	
TRANSISTORS	Q16	
TRANSFORMERS	T3	
CONNECTORS	P4	
SWITCHES	S1	
I C	Z6	
OPTO ISOLATORS	OC2	
INDUCTORS	L3	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIODES ARE 1N914
2. CAPACITOR VALUES ARE IN MICROFARADS, uF
3. RESISTOR VALUES ARE IN OHMS, Ω
4. ⓒ INDICATES TEST POINTS
5. RESISTORS ARE ± 5%, 1/4W

REVISIONS					
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		P	LIMITED USAGE RELEASE			
		A1	REVISED	JDC	8-1-80	
		A4	REVISED PER E.O. 2-10179		9-22-80	
		B	PRODUCTION RELEASE PER E.O. 2-10403		12-7-80	
		D	REVISED PER E.O. 2-10532		2-23-81	
		E	REVISED PER E.O.2-10577		3/27/81	
		D	REVISED PER E.O.2-10696		6-2-81	
		E	REVISED PER E.O.2-10723		7-28-81	
		F	REVISED PER E.O. 2-10936		2/3/82	
		G	REVISED PER E.O.2-11060		4/19/82	
		H	REVISED PER E O 2-11181	JDC	4/9/83	
		B	REVISED PER E.O. 2-11387		9/21/84	

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ASSEMBLY NO. 231-4500-03	SUPERSEDES	
DES/ENG	Greg Schaffer	6-23-80
DRAWN	GLORIA RUIZ	6-14-80
CHECK	Greg Schaffer	6-23-80
APPR.		

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TITLE: SCHEMATIC POWER SUPPLY

SIZE	DRAWING NO.	CHANGE LETTER
D	231-6500-02	B

SCALE: DO NOT SCALE DRAWING — SHEET 1 OF 1

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ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	DATE [illegible]	SHEET 4 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, POWER SUPPLY	231-2500-03	1	
2	SCHEMATIC	231-6500-02	1	
3	TEST SPEC		1	
4				
5				
6				
7	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
8	IC, 4049 HEX INV CMOS (FC,MO)	965-5740-03	1	Z2
9	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z3
10	IC, LM3086 5 XSTR ARRAY (NL)	965-631-00	1	Z1
11	IC, -12V REG., LM320LZ-12 (NL)	965-551-03	1	Z5
12	IC, +12V REG., LM78L12ACZ (NL)	965-551-04	1	Z6
13				
14				
15				
16	RES, FILM RN60C, 1.0K	920-410-01	1	R8
17	RES, FILM RN60C, 2.61K	920-426-11	1	R6
18	RES, CARBON 1/4W ± 5%, 10	942-201-00	2	R52,R39
19	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R47,R37
20	RES, CARBON 1/4W ± 5%, 1K	942-201-02	3	R49,R25,R23,.
21	RES, CARBON 1/4W ± 5%, 10K	942-201-03	4	R26,R27,R28,R2
22	RES, CARBON 1/4W ± 5%, 100K	942-201-04	4	R16,R15,R19,R3
23	RES, CARBON 1/4W ± 5%, 1M	942-201-05	4	R20,R18,R17,R13
24	RES, CARBON 1/4W ± 5%, 120K	942-201-24	1	R9

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ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	DATE 4-13-80	SHEET 5 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ± 5%, 150	942-201-51	1	R1
26	RES, CARBON 1/4W ± 5%, 15K	942-201-53	3	R22,R21,R24
27	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	1	R48
28	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R12,R38
29	RES, CARBON 1/4W ± 5%, 33	942-203-30	4	R29-R32
30	RES, CARBON 1/4W ± 5%, 330	942-203-31	1	R4
31	RES, CARBON 1/4W ± 5%, 47	942-204-70	1	R51
32	RES, CARBON 1/4W ± 5%, 470	942-204-71	2	R35,R36
33	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	2	R14,R5
34	RES, CARBON 1/4W ± 5%, 470K	942-204-74	2	R44,R43
35	RES, CARBON 1/4W ± 5%, 56K	942-205-63	1	R34
36	RES, CARBON 1/2W ± 5%, 1	942-301-00	1	R54
37	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	1	R50
38	RES, CARBON 1/2W ± 5%, 3.0	942-303-09	1	R53
39	RES, CARBON 1/2W ± 5%, 330K	942-303-34	1	R45
40	RES, CARBON 1/2W ± 5%, 470K	942-304-74	1	R46
41	RES, WW, 3W ± 5%, 2	942-602-00	2	R42,R41
42	RES NETWORK 15K SIP 764-3-R15K	950-015-02	1	RN1
43	RES, CARBON 1/4W ± 5%, 8.2K	942-208-22	2	R11,R55
44	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	1	R40
45	RES, CARBON 1/2W ± 5%, 1K	942-301-02	1	R33
46				
47				
48	CAP, .1MF@50V(3429-050E-104Z)A	900-021-02	1	C12

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ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	DATE [illegible]	SHEET 6 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	CAP, DISC, .01 @ 500V (5GA)	900-021-04	3	C28,C3,C1
50	CAP, DISC,.001 @ 1KV (5GA)	900-081-03	2	C29,C2
51	CAP, .1 @ 50V, VARADYNE 1802Z5U	900-021-08	2	C20,C23
52	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	3	C8,C9,C30
53	CAP, ELT, 100/20V SPRG 672D-CG5	910-100-20	1	C21
54	CAP, ELT 180/12V SPRG 672D-CG5	910-180-12	1	C15
55	CAP, ELCTLT, 85@ 150V (39D)	910-851-50	1	C7
56	CAP, ELCTLT 90/200V (39D)	910-902-00	2	C27,C26
57	CAP, ELCTLT 1000/6.3V	910-100-06	1	C17
58	CAP, DISC, .01MF @ 1KV	900-021-05	1	C32
59	CAP, MICA 1200 PF (CD15-FA122GO3)	915-031-22	1	C6
60	CAP, TANT 2.2 @ 35V(196D)	916-220-04	1	C13
61	CAP,.001 @ 50V, VARADYNE 1801X7R	900-021-09	1	C5
62	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C11,C10,C4
63	CAP, .1 250V SF SIEMENS (B32570)	918-001-25	1	C14
64	CAP, 1 100V SF SIEMENS(B32571)	918-010-10	3	C16,C22,C19
65	CAP, MYLAR, .1 @ 400V (ZA2E)	912-010-40	1	C18
66	CAP, DISC, 470pF @ 1KV (5GA)	901-014-71	1	C31
67	CAP, TANT 1µf @ 25V (162D)	916-001-25	1	C33
68				
69				
70	DIODE, 1N457A (LOLEAK)(TD,FC)	961-045-70	2	CR6,CR7
71	DIODE, 1N759 (12V) (TD,MO)	961-075-90	1	CR5
72	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	17	CR2,4,9,11-13, 15.18-21.37-40 42,43

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DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	DATE 4-15-80	SHEET 7 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	DIODE, 1N4933(1A/50V,FAST)(MO)	961-493-30	4	CR27-30
74	DIODE, 1N4937(1A/600V,FAST) MO	961-493-70	5	CR14,16,41,44,45
75	DIODE, 8069 DCQ INTERSIL	961-501-02	1	CR1
76	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
77	DIODE, 1N5232 B 5.6V	961-523-22	2	CR17,CR26
78	DIODE, 1N5270B 91V	961-527-02	2	CR8,CR36
79				
80				
81				
82				
83	POT 5K CERMET (72XL)	960-015-11	1	R10
84	TRANSFORMER, INVERTER	231-7000-00	1	T1
85	TRANSFORMER, SWITCHING	230-7020-01	1	T3
86	TRANSFORMER, PULSE	230-7022-00	1	T2
87	POT, 1K CERMET (72XL)	960-011-25	1	R7
88	XSTR PN2222 (NPN) (NA)	962-222-20	3	Q13,Q14,Q15
89	XSTR, PN2907 (PNP) (NSC)	962-290-70	1	Q1
90	XSTR, 2N4250 (PNP) (FC,NL)	962-425-00	1	Q2
91	SCR, 2N4441 (8A PLASTIC)(MO)	962-444-10	1	Q12
92	XSTR, 92PU01A(NL)	964-040-01	2	Q5,Q7
93	XSTR, 92PU10(NL)	964-040-10	2	Q4,Q9
94	XSTR, 92PU51A (NL)	964-040-51	2	Q6,Q8
95	XSTR, MPSA92 (PNPA) (MO)	964-040-92	1	Q3
96	XSTR, MJE13005	964-130-05	3	Q10,Q11,Q16

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DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	DATE 4-15-80	SHEET 8 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	OPTO FCD 825B (FC)	965-570-08	1	OC2
98	RECTIFIER, 1N4005 600V 1A(DI)	966-002-04	6	CR10,CR31-35
99	RECTIFIER, FAST 3AMP 50V	966-002-08	4	CR22-25
100	CHOKE, 50 MICROHENRY	967-005-14	2	L1,L3
101	HP5082-4350 6N135 OPTO ISO	965-570-00	1	OC1
102	SVP, 270V SMS B2-B270	967-006-01	1	SG2
103	SVP, 470V SMS B2-B470	967-006-02	1	SG1
104	WFR ASSY, 7CKT(09-75-1071)MOLEX	973-070-12	1	P2
105	WFR ASSY, 6CKT(09-75-1061)MOLEX	973-070-11	1	P3
106	HEAT SINK, THERMALLY THM6073	991-008-00	3	HS1-HS3
107	WFR ASSY, 2CKT(09-75-1021)MOLEX	973-070-25	1	P4
108	INDUCTOR, 5.6UH, CAMBION	967-005-02	1	L2
109	SHIELD, POWER SUPPLY	231-2630-00	1	
110	CHASSIS FSNR 632B2(US1590B1)	991-020-26	1	
111	SCREW, PAN HD PHILLIPS, 4-40 X 3/8	980-440-038	4	
112	SCREW, NYLON PAN HD SLOT 6-32 X 15/16	983-632-0937	1	
113	SCREW, NYLON PAN HD SLOT 4-40 X 1/2	983-440-050	1	
114	SCREW, PAN HD PHILLIPS, 6-32 X 5/16	980-632-031	3	
115	HEX NUT 4-40	984-100-440	1	
116	HEX NUT 6-32	984-100-632	1	
117	HEX NUT, RADIAL 6-32	984-200-632	3	
118	WASHER, SPLITLOCK 4	986-200-04	4	
119	WASHER, SPLITLOCK 6	986-200-06	3	
120	WASHER, FLAT NYLON 4	986-800-00	1	

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	231-4500-03	B
		DATE 8-20-80	SHEET 9 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
121	WASHER, FLAT NYLON 6	986-800-04	1	
122	WASHER, INT STAR 4	986-400-04	1	
123	WASHER, INT STAR 6	986-400-06	1	
124	LABEL, HI-VOLTAGE (T&B#WCSS76F)	991-060-10	1	
125	JUMPER, J.500X.125T22	991-010-05	3	JMP 1 - JMP 3

(11) INSTALL A SLEEVED 20 GA. BUS WIRE HOLD-DOWN AROUND C7,C26, & C27.

(12) INSTALL TRANSFORMER AFTER AQUEOUS WASH.

(13) INSTALL 1" SPONGE STRIPS (ITEM 127) ON TRANSFORMER AS SHOWN.

(5) INSTALL HARDWARE AS NOTED:
SCREW, NYLON 4-40 X 1/2" (983-440-050)
WASHER, FLAT NYLON (986-800-00)
STAR WASHER, #4 (986-400-04)
NUT, #4 (984-100-440)

(6) RUBBER STAMP ASSY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR (CIRCUIT) SIDE.

(7) INSTALL ON THIS SIDE CHASSIS FASTENER 991-020-26. THREADED HOLE TO BE ORIENTED AS SHOWN.

(8) INSTALL Q12 WITH METAL TAB FACING UP P/N 962-444-10.

(9) REMOVE PINS 1 & 3 ON P2.

(10) REMOVE PIN 4 ON P3.

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.

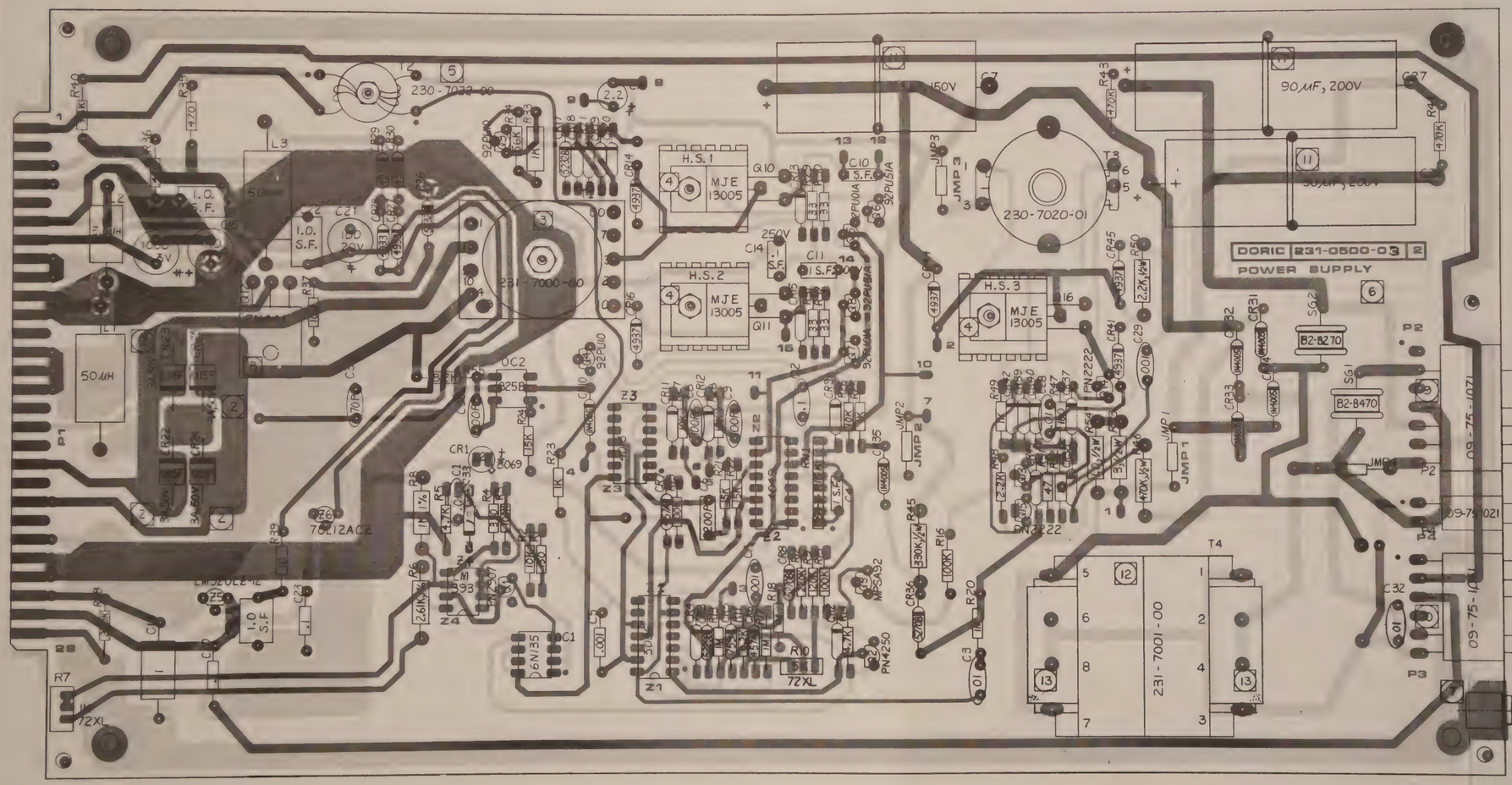
(2) MOUNT COMPONENT 1/8" OFF P.C. BOARD.

(3) INSTALL HARDWARE AS NOTED:
SCREW, NYLON 6-32 X 15/16" (983-632-0937)
WASHER, FLAT, NYLON (986-800-04)
STAR WASHER #6 (986-400-06)
NUT, HEX #6 (984-100-632)

(4) INSTALL HARDWARE AS NOTED:
SCREW, 6-32 X 5/16" (980-632-031)
WASHER, SPLITLOCK #6 (986-200-06)
NUT, RADIAL #6 (984-200-632)
HEATSINK (991-008-00)

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		B	PRODUCTION RELEASE PER E.O. 2-10628	JDC	10/30/81	J. Crabtree
		C	REVISED PER E.O. 2-10936	JDC	2/12/82	DWS
		D	REVISED PER E.O. 2-10999	JB	9-27-82	[illegible]
		E	REVISED PER E.O. 2-11060	JB	9-27-82	[illegible]
		F	REVISED PER E.O. 2-11240	JC	7/19/83	J. Crabtree
		G	REVISED PER E.O. 2-11241	JC	7/19/83	J. Crabtree
		B	REVISED PER E.O. 2-11387	HL	6/2/84	J. Crabtree



HOLE TOLERANCES	NOTES UNLESS SPECIFIED	DRAWN	H. LAM	8-3-81
.005-.250 DIA +.004-.002 .251-.500 DIA +.006-.002 .501-1.00 DIA +.010-.005	1. TOLERANCES .XX ± .03 DIMENSIONED ANGLES .XXX ± .010 ± ½° 2. BREAK ALL SHARP EDGES .010 APPROX. 3. MACH. SURFACES 4. ALL DIM. IN INCHES 5. ALL TRUE POSITION TOLERANCES APPLY AT MMC	CHECK	J. Crabtree	10/30/81
SUPERSEDES		APPR.	T. Pinder	10/30/81
		MATERIAL		
	USED ON. 235	FINISH		
	NEXT ASSY. 231-0000-XX			

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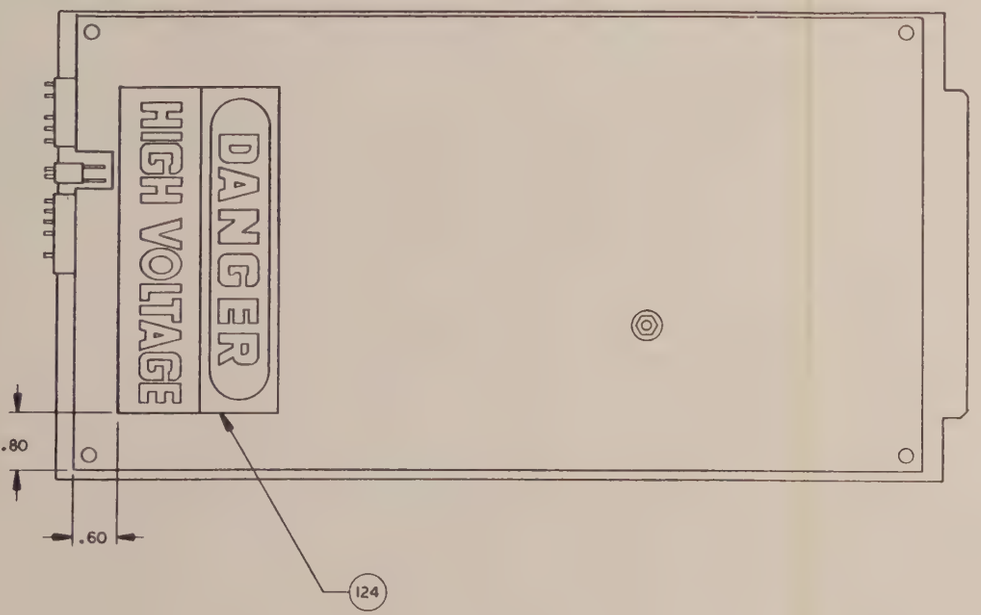
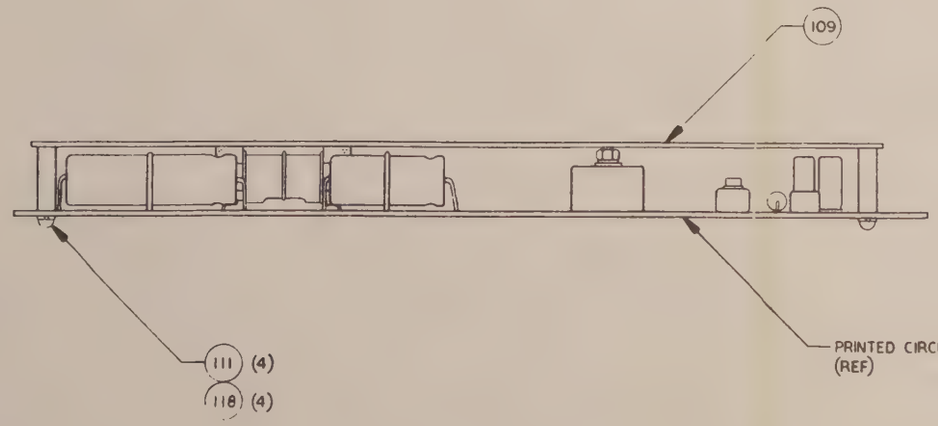
TITLE: ASSEMBLY P.C.B., POWER SUPPLY 100 VAC

SIZE	CODE IDENT. NO.	DRAWING NO.	CHANGE LETTER
D		231-4501-01	B

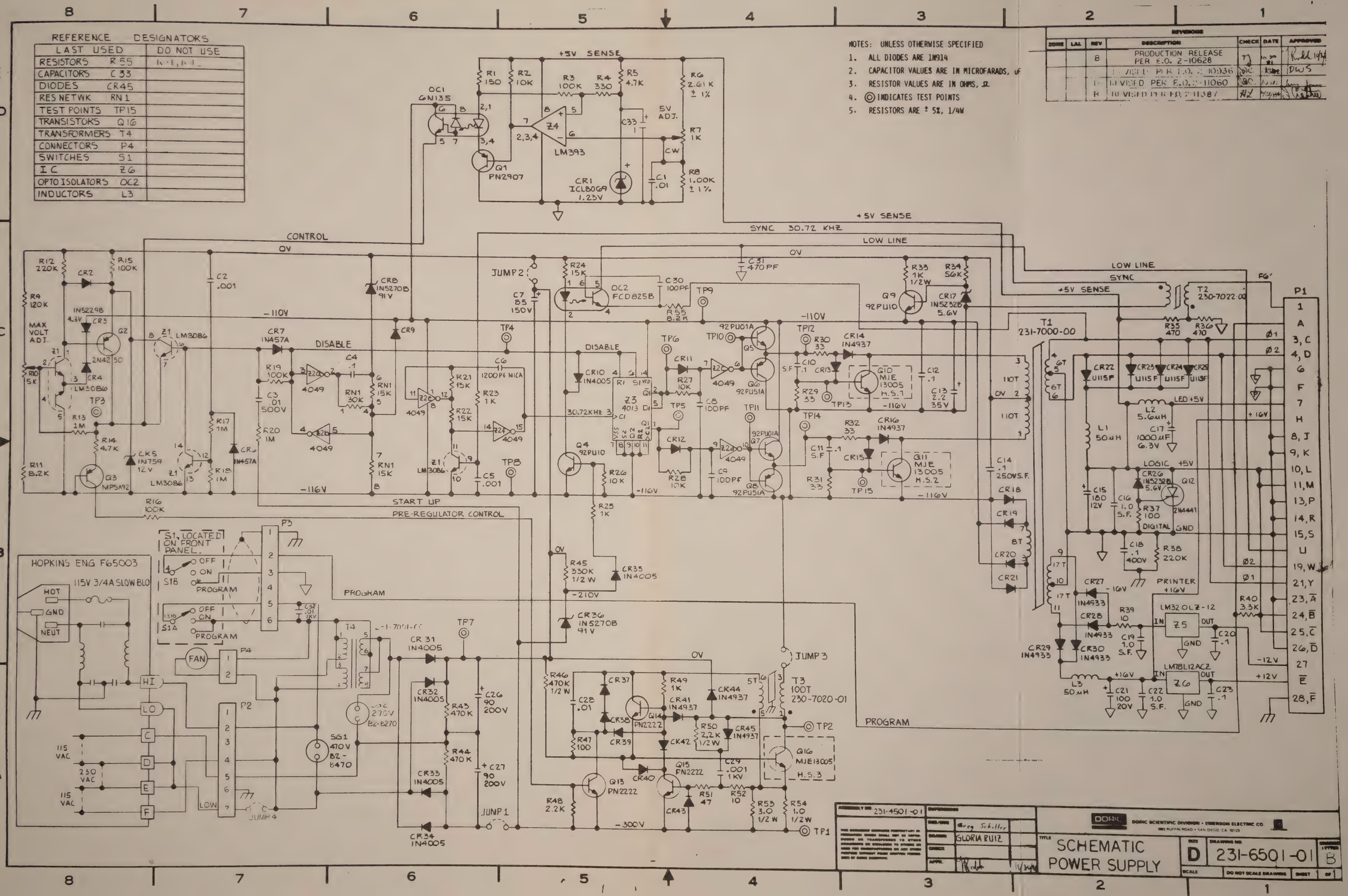
SCALE 1:1 | DO NOT SCALE DRAWING | SHEET 1 OF 9

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED





SIZE	CODE IDENT. NO.	DRAWING NO.	CHANGE LETTER
D		231-4501-01	B
SCALE 1:1	DO NOT SCALE DRAWING	SHEET 2 OF 9	



REFERENCE DESIGNATORS
LAST USED | DO NOT USE
RESISTORS R55
CAPACITORS C33
DIODES CR45
RES NETWK RN1
TEST POINTS TP15
TRANSISTORS Q16
TRANSFORMERS T4
CONNECTORS P4
SWITCHES S1
IC Z6
OPTO ISOLATORS OC2
INDUCTORS L3
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE 1N914
2. CAPACITOR VALUES ARE IN MICROFARADS, uF
3. RESISTOR VALUES ARE IN OHMS, Ω
4. ◎ INDICATES TEST POINTS
5. RESISTORS ARE ± 5%, 1/4W
REVISIONS
ZONE | LAL | REV | DESCRIPTION | CHECK | DATE | APPROVED
B | PRODUCTION RELEASE PER E.O. 2-10628
REVISED PER E.O. 2-10936
REVISED PER E.O. 2-11060
REVISED PER E.O. 2-11387
+5V SENSE
SYNC 30.72 KHZ
LOW LINE
CONTROL
0V
-110V
DISABLE
START UP
PRE-REGULATOR CONTROL
PROGRAM
HOPKINS ENG F65003
115V 3/4A SLOW BLO
HOT
GND
NEUT
S1, LOCATED ON FRONT PANEL.
OFF
ON
PROGRAM
FAN
115 VAC
230 VAC
115 VAC
LOW
JUMP 1
JUMP 2
JUMP 3
JUMP 4
T1 231-7000-00
T2 230-7022-00
T3 100T 230-7020-01
T4
LOGIC
DIGITAL
PRINTER
+16V
-12V
+12V
-210V
-300V
P1
P2
P3
P4
ASSEMBLY NO. 231-4501-01
DRAWN Greg Schiller
GLORIA RUIZ
DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
SCHEMATIC POWER SUPPLY
D
231-6501-01
B
DO NOT SCALE DRAWING

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, POWER SUPPLY 100VAC	MODEL NO. 235	DATE 8-5-81	SHEET 4 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, POWER SUPPLY	231-2500-03	1	
2	SCHEMATIC	231-6501-01	1	
3	TEST SPEC		1	
4				
5				
6				
7	IC, LM393 DUAL COMP (8DIP) (NL)	965-580-00	1	Z4
8	IC, 4049 HEX INV CMOS (FC, MO)	965-5740-03	1	Z2
9	IC, 4013 DUAL D FF CMOS (FC, MO)	965-587-23	1	Z3
10	IC, LM3086 5 XSTR ARRAY (NL)	965-631-00	1	Z1
11	IC, -12V REG., LM320LZ-12 (NL)	965-551-03	1	Z5
12	IC, +12V REG., LM78L12ACZ (NL)	965-551-04	1	Z6
13				
14				
15				
16	RES, FILM RN60C, 1.0K	920-410-01	1	R8
17	RES, FILM RN60C, 2.61K	920-426-11	1	R6
18	RES, CARBON 1/4W ±5%, 10	942-201-00	2	R52, R39
19	RES, CARBON 1/4W ±5%, 100	942-201-01	2	R47, R37
20	RES, CARBON 1/4W ±5%, 1K	942-201-02	3	R49,25,23,
21	RES, CARBON 1/4W ±5%, 10K	942-201-03	4	R26,27,28,R2
22	RES, CARBON 1/4W ±5%, 100K	942-201-04	4	R16,15,19,R3
23	RES, CARBON 1/4W ±5%, 1M	942-201-05	4	R20,18,17,13
24	RES, CARBON 1/4W ± 5%, 120K	942-201-24	1	R9

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, POWER SUPPLY 100VAC	MODEL NO. 235	DATE 8-5-81	SHEET 5 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ±5%, 150	942-201-51	1	R1
26	RES, CARBON 1/4W ±5%, 15K	942-201-53	3	R22,21,24
27	RES, CARBON 1/4W ±5%, 2.2K	942-202-22	1	R48
28	RES, CARBON 1/4W ±5%, 220K	942-202-24	2	R12,38
29	RES, CARBON 1/4W ±5%, 33	942-203-30	4	R29-32
30	RES, CARBON 1/4W ±5%, 330	942-203-31	1	R4
31	RES, CARBON 1/4W ±5%, 47	942-204-70	1	R51
32	RES, CARBON 1/4W ±5%, 470	942-204-71	2	R35, 36
33	RES, CARBON 1/4W ±5%, 4.7K	942-204-72	2	R14,5
34	RES, CARBON 1/4W ±5%, 470K	942-204-74	2	R44,43
35	RES, CARBON 1/4W ±5%, 56K	942-205-63	1	R34
36	RES, CARBON 1/2W ±5%, 1	942-301-00	1	R54
37	RES, CARBON 1/2W ±5%, 2.2K	942-302-22	1	R50
38	RES, CARBON 1/2W ±5%, 3.0	942-303-09	1	R53
39	RES, CARBON 1/2W ±5%, 330K	942-303-34	1	R45
40	RES, CARBON 1/2W ±5%, 470K	942-304-74	1	R46
41				
42	RES, NTWK 15K SIP 764-3-R15K	950-015-02	1	RN1
43	RES, CARBON 1/4W ±5%, 8.2K	942-208-22	2	R11,55
44	RES, CARBON 1/4W ±5%, 3.3K	942-203-32	1	R40
45	RES, CARBON 1/2W ±5%, 1K	942-301-02	1	R33
46				
47				
48	CAP, .1MF @ 50V(3429-050E-104Z)A	900-021-02	1	C12

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, POWER SUPPLY 100VAC	MODEL NO. 235	DATE 8-5-81	SHEET 6 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	CAP, DISC, .01 @ 500V (5GA)	900-021-04	3	C28,3,1
50	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C29, 2
51	CAP, .1 @ 50V, VARADYNE 1802Z5U	900-021-08	2	C20, C23
52	CAP, DISC, 100PF @ 1KV (5GA)	901-011-01	3	C8,C9,C30
53	CAP, ELT, 100/20V SPRG 672D-CG5	910-100-20	1	C21
54	CAP, ELT 180/12V SPRG 672D-CG5	910-180-12	1	C15
55	CAP, ELCTLT, 85 @ 150V (39D)	910-851-50	1	C7
56	CAP, ELCTLT 90/200V (39D)	910-902-00	2	C27,C26
57	CAP, ELCTLT 1000/6.3V	910-100-06	1	C17
58	CAP, DISC, .01MF @ 1KV	900-021-05	1	C32
59	CAP, MICA 1200 PF (CD15-FA122G03)	915-031-22	1	C6
60	CAP, TANT 2.2 @ 35V (196D)	916-220-04	1	C13
61	CAP, .001 @ 50V, VARADYNE 1801X7R	900-021-09	1	C5
62	CAP, SF, .1/100V, SMS(B32570)	918-001-10	3	C11,10,4
63	CAP, .1 250V SF SIEMENS (B32570)	918-001-25	1	C14
64	CAP, 1 100V SF SIEMENS (B32571)	918-010-10	3	C16,22,19
65	CAP, MYLAR, .1 @ 400V (ZA2E)	912-010-40	1	C18
66	CAP, DISC, 470pF @ 1KV (5GA)	901-014-71	1	C31
67	CAP, TANT 1µf @ 25V (162D)	916-001-25	1	C33
68				
69				
70	DIODE, 1N457A (LOLEAK)(TD,FC)	961-045-70	2	CR6,CR7
71	DIODE, 1N759 (12V) (TD,MO)	961-075-90	1	CR5
72	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	17	CR2,4,9,11-13, 15,18-21,37-40,42, 43

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, POWER SUPPLY 100VAC	MODEL NO. 235	231-4501-01	B
		DATE 8-5-81	SHEET 7 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	DIODE, 1N4933(1A/50V,FAST)(MO)	961-493-30	4	CR27-30
74	DIODE, 1N4937(1A/600V,FAST)(MO)	961-493-70	5	CR14,16,41,44,45
75	DIODE, 8069 DCQ INTERSIL	961-501-02	1	CR1
76	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
77	DIODE, 1N5232 B 5.6V	961-523-22	2	CR17,CR26
78	DIODE, 1N5270B 91V	961-527-02	2	CR8,CR36
79				
80				
81				
82	TRANSFORMER, PRINTED CIRCUIT	231-7001-00	1	T4
83	POT, 5K CERMET (72XL)	960-015-11	1	R10
84	TRANSFORMER, INVERTER	231-7000-00	1	T1
85	TRANSFORMER, SWITCHING	230-7020-01	1	T3
86	TRANSFORMER, PULSE	230-7022-00	1	T2
87	POT, 1K CERMET (72XL)	960-011-25	1	R7
88	XSTR PN2222 (NPN)(NA)	962-222-20	3	Q13,14,15
89	XSTR, PN2907 (PNP)(NSC)	962-290-70	1	Q1
90	XSTR, 2N4250 (PNP)(FC,NL)	962-425-00	1	Q2
91	SCR, 2N4441 (8A PLASTIC)(MO)	962-444-10	1	Q12
92	XSTR, 92PU01A (NL)	964-040-01	2	Q5,Q7
93	XSTR, 92PU10 (NL)	964-040-10	2	Q4,Q9
94	XSTR, 92PU51A (NL)	964-040-51	2	Q6,Q8
95	XSTR, MPSA92 (PNPA) (MO)	964-040-92	1	Q3
96	XSTR, MJE13005	964-130-05	3	Q10,11,16

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, POWER SUPPLY 100VAC		231-4501-01	B
	MODEL NO. 235	DATE 8-5-81	SHEET 8 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	OPTO FCD 825B (FC)	965-570-08	1	OC2
98	RECTIFIER, 1N4005 600V 1A (DI)	966-002-04	6	CR10,CR31-35
99	RECTIFIER, FAST 3 AMP 50V	966-002-08	4	CR22-25
100	CHOKE, 50 MICROHENRY	967-005-14	2	L1,L3
101	HP5082-4350 6N135 OPTO ISO	965-570-00	1	OC1
102	SVP, 270V SMS B2-B270	967-006-01	1	SG2
103	SVP, 470V SMS B2-B470	967-006-02	1	SG1
104	WFR ASSY, 7CKT(09-75-1071)MOLEX	973-070-12	1	P2
105	WFR ASSY, 6CKT(09-75-1061)MOLEX	973-070-11	1	P3
106	HEATSINK, THERMALLY THM6073	991-008-00	3	HS1-HS3
107	WFR ASSY, 2CKT(09-75-1021)MOLEX	973-070-25	1	P4
108	INDUCTOR, 5.6UH, CAMBION	967-005-02	1	L2
109	SHIELD, POWER SUPPLY	231-2630-00	1	
110	CHASSIS, FSNR 632B2(US1590B1)	991-020-26	1	
111	SCREW, PAN HD PHILLIPS, 4-40 X 3/8	980-440-038	4	
112	SCREW, NYLON PAN HD SLOT 6-32 X 15/16	983-632-0937	1	
113	SCREW, NYLON PAN HD SLOT 4-40 X 1/2	983-440-050	1	
114	SCREW, PAN HD PHILLIPS, 6-32 X 5/16	980-632-031	3	
115	HEX NUT 4-40	984-100-440	1	
116	HEX NUT 6-32	984-100-632	1	
117	HEX NUT, RADIAL 6-32	984-200-632	3	
118	WASHER, SPLITLOCK 4	986-200-04	4	
119	WASHER, SPLITLOCK 6	986-200-06	4	
120	WASHER, FLAT NYLON 4	986-800-00	1	

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, POWER SUPPLY 100VAC	MODEL NO. 235	DATE 8-5-81	SHEET 9 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
121	WASHER, FLAT NYLON 6	986-800-04	1	
122	WASHER, INT STAR 4	986-400-04	1	
123	WASHER, INT STAR 6	986-400-06	1	
124	LABEL, HI-VOLTAGE (T&B#WCSS76P)	991-060-10	1	
125	JUMPER, J.500X .125T22	991-010-05	3	JMP 1 - JMP 3
126	JUMPER, J.600X .125T22	991-010-06	1	JMP 4
127	SPONGE, ADHESIVE BACK #401 1/4 X 7/16	976-100-51	2"	(2) 1" STRIPS
128	SCREW, PHMS, 6-32 X 1/2	980-632-050	1	
129	WASHER FLAT NO. 6	986-100-06	1	
130				
131				
132				
133				
134				
135				
136				
137				
138				
139				
140				
141				
142				
143				
144				

6 INSTALL JUMPER (ITEM 96) ACROSS TP12 & TP13.

7 DELETED.

8 INSTALL BATTERY BT1 TO BAORD USING 20 AWG INSULATED BUSS WIRE, 2 PLACES.

9 INSTALL CONNECTOR P2 TO THE BOARD USING 2-56 X 1/2 LG SCREWS, (ITEM 84), NO. 2 SPLITLOCK WASHER, (ITEM 88), AND 2-56 HEX NUT, (ITEM 86), 2 PLACES.

10. FOR MATERIAL LIST, SEE SHEETS 2 THRU 6.

11 INSTALL 24 PIN I.C. SOCKET, (ITEM 95), 1 PLACE.

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.

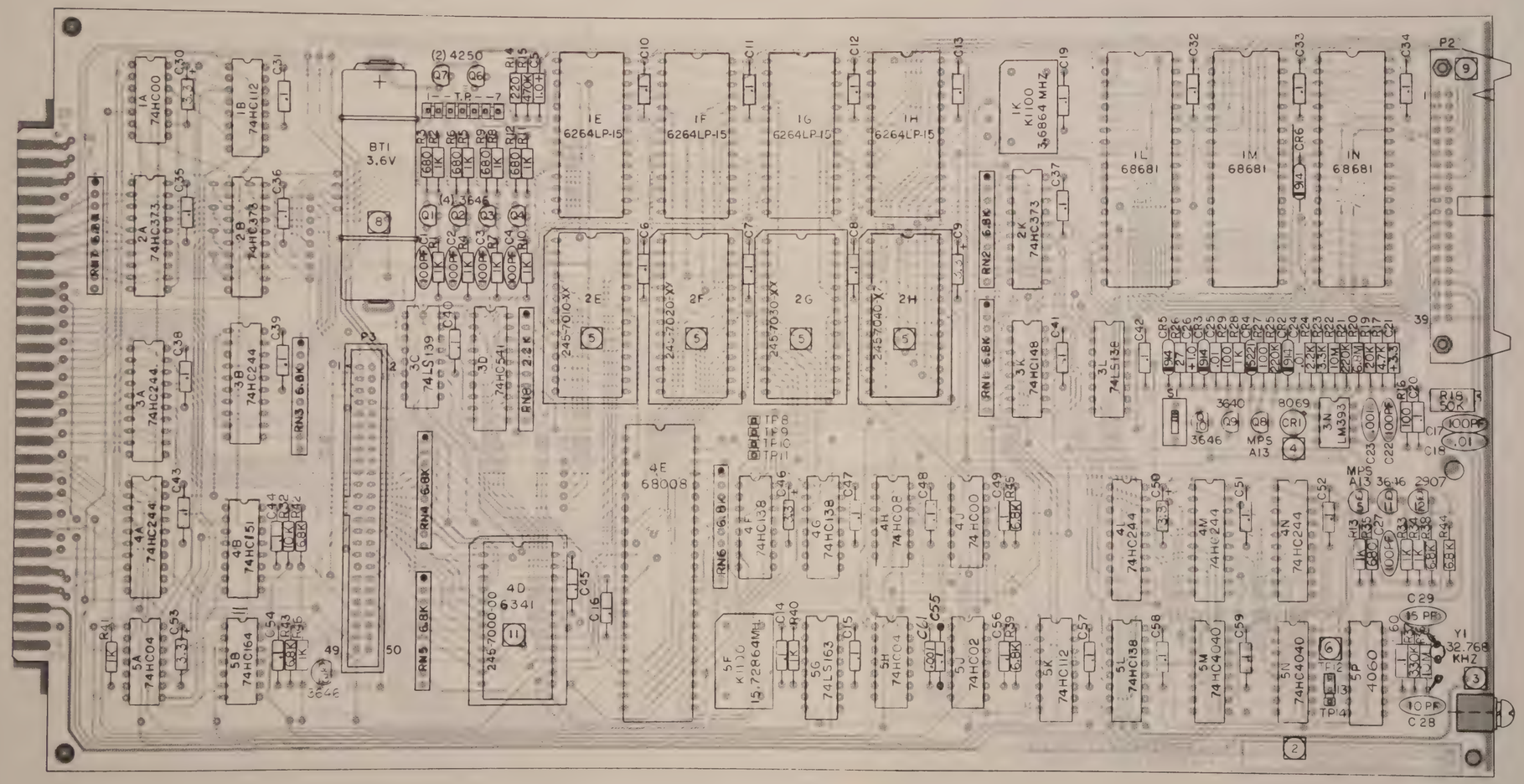
2 RUBBER STAMP ASSEMBLY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR (SOLDER) SIDE.

3 INSTALL CHASSIS FSTNR, (ITEM 90), ON COMPONENT SIDE. ORIENTED AS SHOWN. INSTALL 6-32 X 1/2 LG SCREWS (ITEM 85), NO. 6 SPLITLOCK WASHER (ITEM 89), AND NO. 6 FLAT WASHER, (ITEM 87), INTO CHASSIS FSTNR.

4 MOUNT CR1 (8069) .03 OFF THE BOARD. (USE DISS-O-PAD NO. TO-16-03 OR OTHER ACCEPTABLE METHOD).

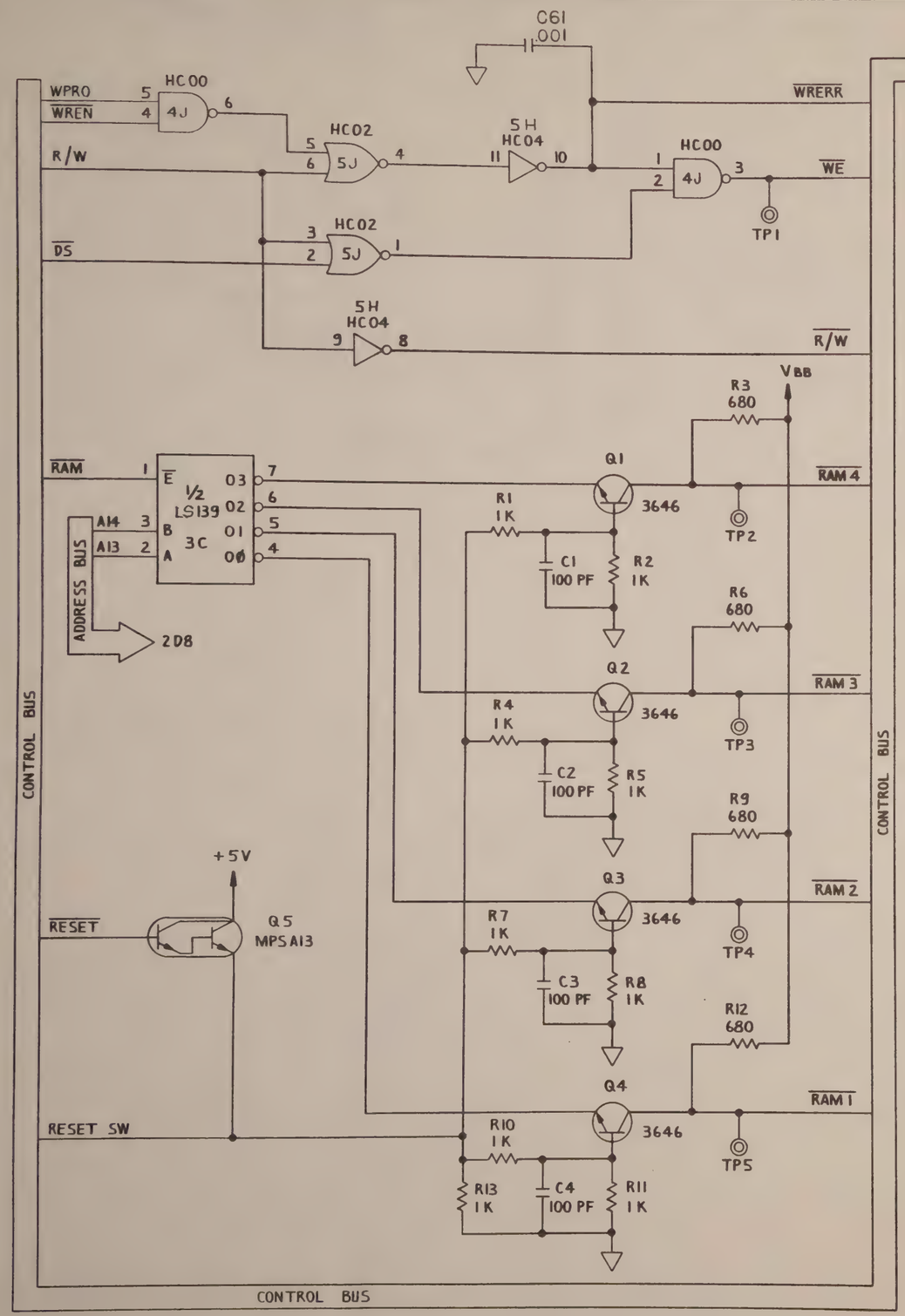
5 INSTALL 28 PIN I.C. SOCKET (ITEM 93), 4 PLACES.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X2	R&D RELEASE		5/7	
		X3	R&D RELEASE			
		A1	LTD USAGE REL PER E.O. 2-11431	J.J.	8/6/84	
		B	PROD. REL. PER E.O. 2-11453	J.J.	9/24/84	
		B	REVISED PER E.O. 11517	H.B.	3/5/85	
		C	REVISED PER EO 2-11551	J.J.	7/11/85	
		B	REVISED PER EO 2-11619	S.D.	9/4/85	



HOLE TOLERANCES	NOTES UNLESS SPECIFIED	DRAWN L.OFTEDAHL 12-9-83	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO, CA 92123
.000-.250 DIA +.004-.002 .251-.500 DIA +.006-.002 .501-1.00 DIA +.010-.005	1. TOLERANCES XX ± .02 DIMENSIONED ANGLES ± .5° XXX ± .010 2. BREAK ALL SHARP EDGES .010 APPROX. 3. MACH. SURFACES 4. ALL DIM. IN INCHES 5. ALL TRUE POSITION TOLERANCES APPLY AT MMC	CHECK APPR 5117 3+ MATERIAL	TITLE ASSEMBLY, PCB, CPU
SUPERSEDES	USED ON 245 NEXT ASSY 245-0000-XX	FINISH	SIZE D · CODE IDENT NO · DRAWING NO 245-4110-02 · CHANGE LETTER B SCALE 2:1 · DO NOT SCALE DRAWING · SHEET 1 OF 6

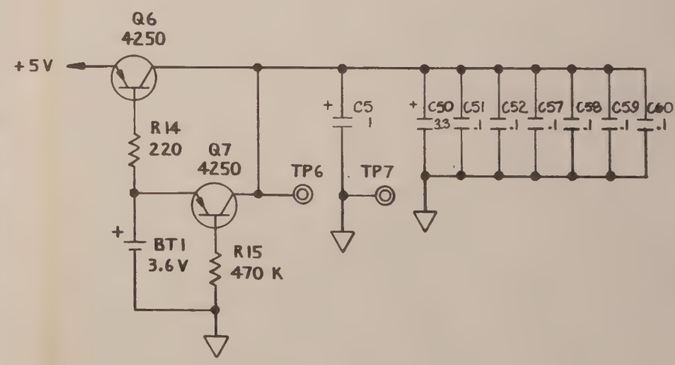
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC



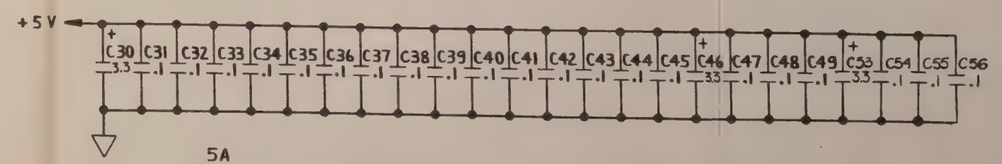
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. DIODES ARE 1N914 OR 1N4148.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X3	R & D RELEASE			
		A1	LTD USAGE REL PER E.O. 2-11431			
		B	PROD. REL. PER E.O. 2-11453			
		B	REVISED PER E.O. 2-11619			



REF DESIGNATORS		
LAST USED		DO NOT USE
RESISTOR	R46	
CAPACITOR	C61	
TRANSISTOR	Q13	
DIODE	CR6	
IC	5P	
BATTERY	BT1	
SWITCH	S1	
TEST POINT	TP14	
RES NETWORK	RN8	
CONN	P3	
CRYSTAL	Y1	



ASSEMBLY NO.

SUPERSEDES

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC.

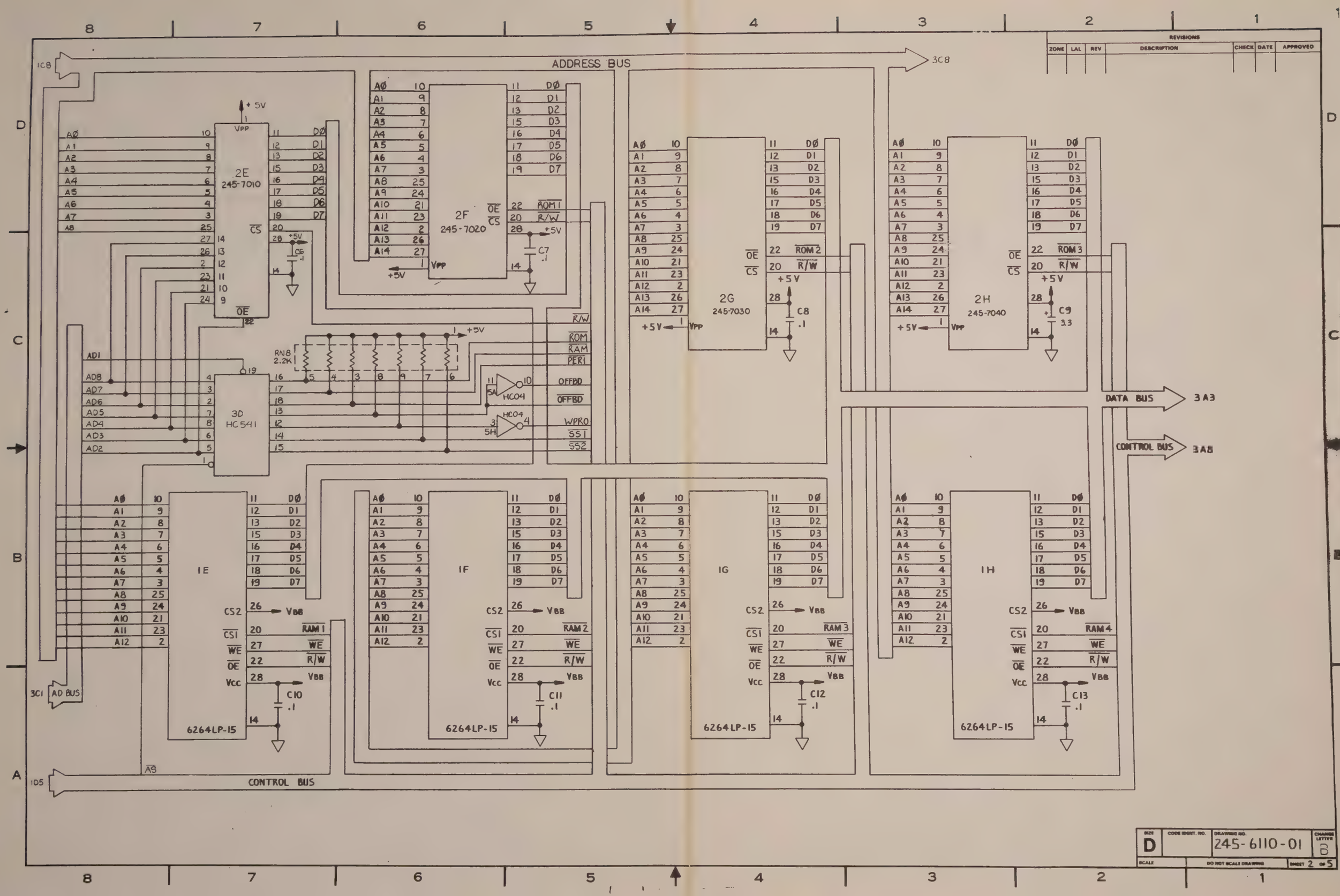
DES/ENG	Terry Jones	5/17/84
DRAWN	S. DUONG	10-12-83
CHECK	Terry Jones	5/17/84
APPR.		

DORIC DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
2863 RUFFIN ROAD • SAN DIEGO, CA 92123

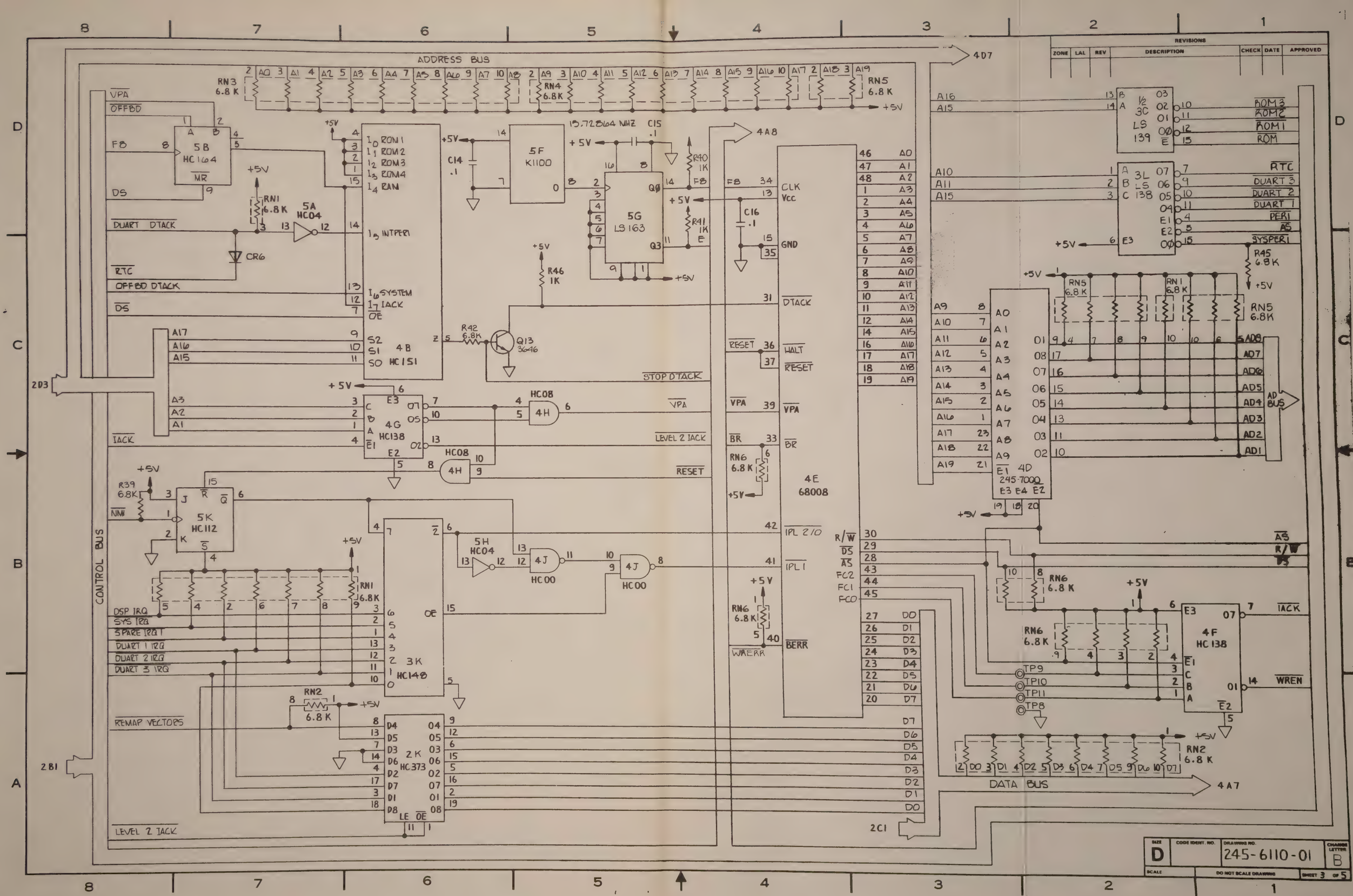
TITLE: SCHEMATIC, CPU BOARD

SIZE	DRAWING NO.	CHANGE LETTER
D	245-6110-01	B

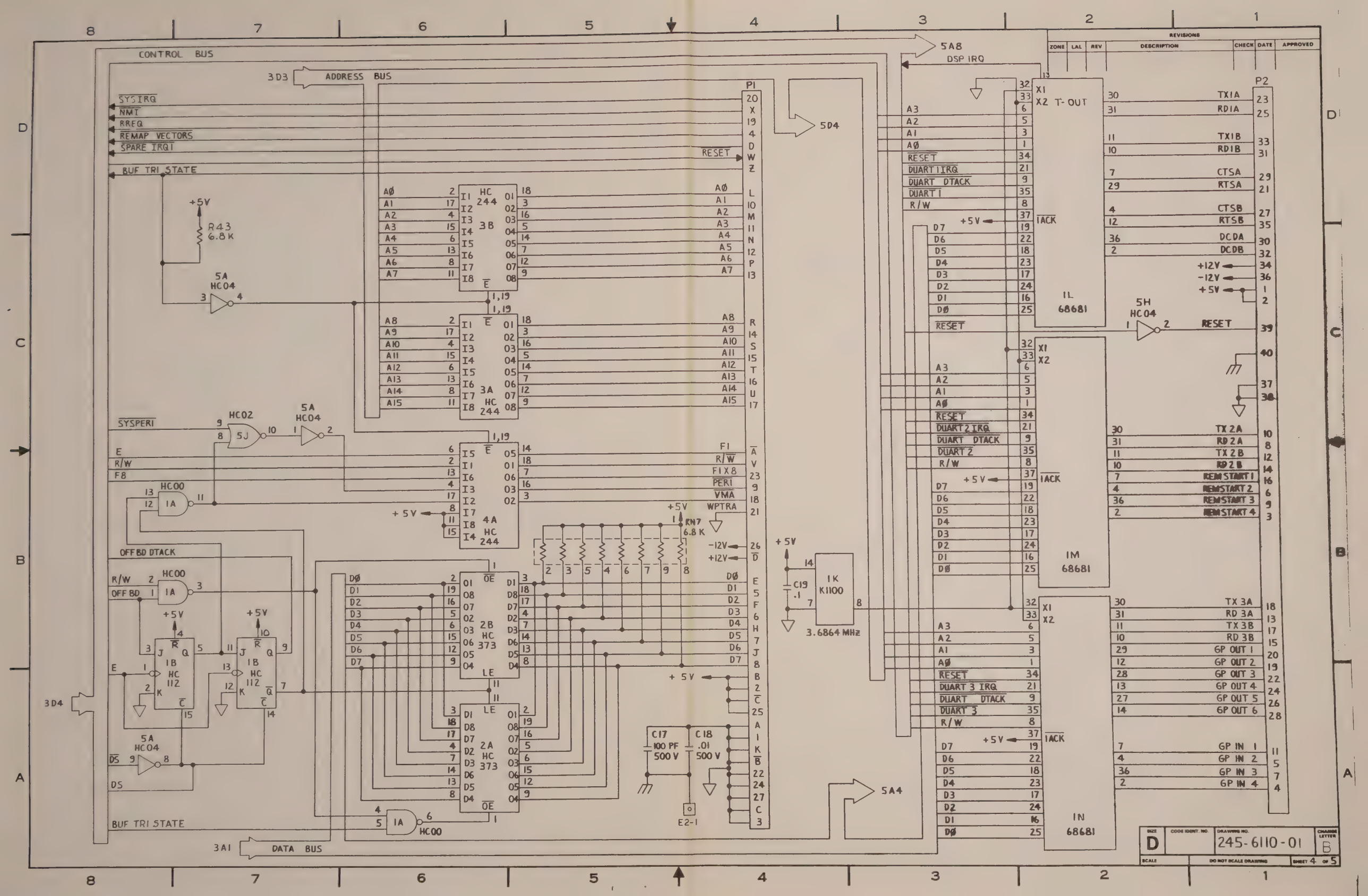
SCALE: DO NOT SCALE DRAWING SHEET 1 OF 5



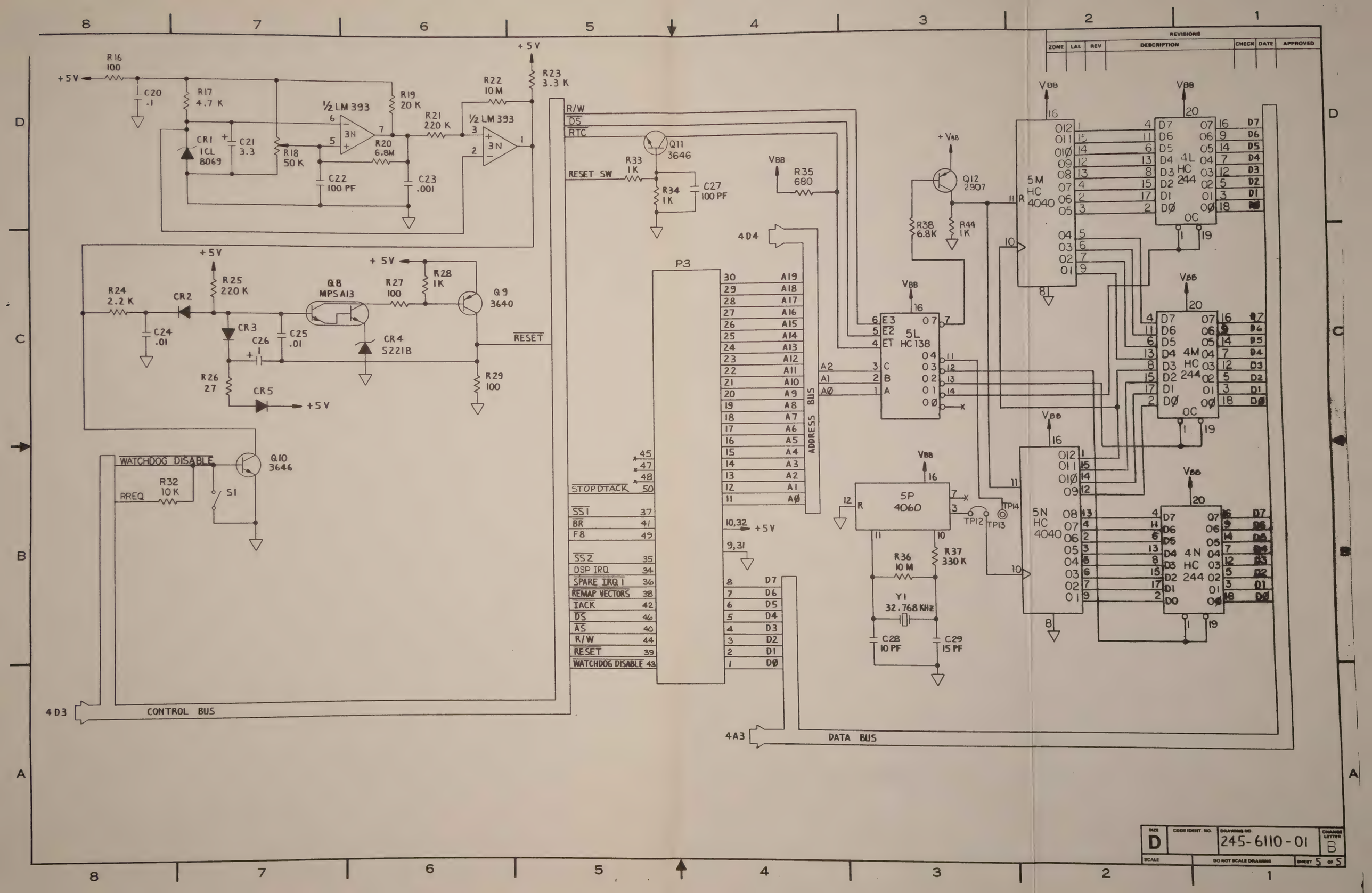
ADDRESS BUS
DATA BUS
CONTROL BUS
AD BUS
2E 245-7010
2F 245-7020
2G 245-7030
2H 245-7040
3D HC541
1E 6264LP-15
1F 6264LP-15
1G 6264LP-15
1H 6264LP-15
RN8 2.2K
HC04
REVISIONS
ZONE LAL REV DESCRIPTION CHECK DATE APPROVED
SIZE D
DRAWING NO. 245-6110-01
CHANGE LETTER B
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 5



ADDRESS BUS
CONTROL BUS
DATA BUS
REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
5B HC164
5A HC04
4B HC151
5F K1100
5G LS163
4G HC138
5K HC112
3K HC148
2K HC373
4E 68008
4D 245-7000
4F HC138
1/2 3C LS 139
3L LS 138
15.72864 MHZ
VPA
OFFBD
F8
DS
DUART DTACK
RTC
OFFBD DTACK
IACK
NMI
DSP IRQ
SYS IRQ
SPARE IRQ
DUART 1 IRQ
DUART 2 IRQ
DUART 3 IRQ
REMAP VECTORS
LEVEL 2 IACK
STOP DTACK
LEVEL 2 IACK
RESET
WRERR
BERR
IPL 2/0
IPL 1
ROM3
ROM2
ROM1
ROM
RTC
DUART 3
DUART 2
DUART 1
PERI
AS
SYSPERI
IACK
WREN
AD BUS
SIZE
D
CODE IDENT. NO.
DRAWING NO.
245-6110-01
CHANGE LETTER
B
SCALE
DO NOT SCALE DRAWING
SHEET 3 OF 5



CONTROL BUS
ADDRESS BUS
DATA BUS
SYSIRQ
NMI
RREQ
REMAP VECTORS
SPARE IRQ1
BUF TRI STATE
SYSPERI
OFF BD DTACK
OFF BD
DSP IRQ
T-OUT
IL 68681
IM 68681
IN 68681
3.6864 MHz
R43 6.8K
RN7 6.8K
C17 100 PF 500 V
C18 .01 500 V
E2-1
REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
SIZE D
CODE IDENT. NO.
DRAWING NO. 245-6110-01
CHANGE LETTER B
SCALE
DO NOT SCALE DRAWING
SHEET 4 OF 5



REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
R16 100
+5V
C20 .1
R17 4.7 K
CR1 ICL 8069
C21 3.3
R18 50 K
½ LM 393
3N
R19 20 K
R20 6.8M
C22 100 PF
C23 .001
R21 220 K
R22 10 M
R23 3.3 K
R24 2.2 K
CR2
R25 220 K
C24 .01
CR3
C26 1
C25 .01
Q8 MPS A13
R27 100
R28 1K
Q9 3640
CR4 5221B
RESET
R26 27
CR5
R29 100
WATCHDOG DISABLE
Q10 3646
RREQ
R32 10 K
S1
4D3
CONTROL BUS
R/W
DS
RTC
RESET SW
Q11 3646
R33 1K
R34 1K
C27 100 PF
VBB
R35 680
4D4
P3
STOPDTACK
SS1
BR
F8
SS2
DSP IRQ
SPARE IRQ 1
REMAP VECTORS
IACK
DS
AS
R/W
RESET
WATCHDOG DISABLE
ADDRESS BUS
10,32
9,31
+5V
4A3
DATA BUS
Q12 2907
R38 6.8K
R44 1K
5L HC 138
5P 4060
R36 10 M
R37 330 K
Y1 32.768 KHz
C28 10 PF
C29 15 PF
TP12
TP13
TP14
5M HC 4040
5N HC 4040
4L HC 244
4M HC 244
4N HC 244
SIZE
D
CODE IDENT. NO.
DRAWING NO.
245-6110-01
CHANGE LETTER
B
SCALE
DO NOT SCALE DRAWING
SHEET 5 OF 5

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, CPU		245-4110-02	B
	MODEL NO. 245	DATE 12-13-83	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, CPU	245-2110-01	1	
2	SCHEMATIC, CPU	245-6110-01	1	
3	TEST SPEC			
4				
5	IC, 74LS138	965-635-22	1	3L
6	IC, LM393 DUAL COMP (8 DIP)(NL)	965-580-00	1	3N
7	IC, 74HC00 4-2 IN NAND (TI)	965-6351-00	2	1A,4J
8	IC, 74HC373	965-6351-02	3	2A,2B,2K
9	IC, 74HC244	965-6351-03	6	3A,3B, 4A,4L,4M,4N
10	IC, 74HC02	965-6351-04	1	5J
11	IC, 74HC04	965-6351-05	2	5A,5H
12	IC, 74HC08	965-6351-06	1	4H
13	IC, 74HC541	965-6351-18	1	3D
14	IC, 74HC112	965-6351-10	2	1B,5K
15	IC, 74HC138	965-6351-11	3	4F,4G,5L
16	IC, 74LS139	965-635-55	1	3C,
17	IC, 74HC148	965-6351-23	1	3K
18	IC, 74LS163	965-635-49	1	5G
19	IC, 74LS164	965-6350-58	1	5B
20	IC, 74HC151	965-6351-35	1	4B
21	IC, 74HC4040	965-6351-20	2	5M,5N
22	IC, 4060	965-6351-21	1	5P
23	IC, K1100 OSCILLATOR 3.6864 MHz	965-5880-10	1	1K
24	IC, K1100 OSCILLATOR 15.72864 MHz	965-5880-11	1	5F

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, CPU		245-4110-02	B
	MODEL NO. 245	DATE 12-13-83	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	IC, 6264LP-15	965-6100-17	4	1E,1F,1G,1H
26	IC, ADDRESS DECODE PROM	245-7000-01	1	4D
27	IC, MAIN FIRMWARE	245-7010-02	1	2E
28	IC, MAIN FIRMWARE	245-7020-02	1	2F
29	IC, MAIN FIRMWARE	245-7030-02	1	2G
30	IC, MAIN FIRMWARE	245-7040-02	1	2H
31	IC, 68008 MPU	965-5590-04	1	4E
32	IC, 68681 DUART	965-5590-05	3	1L,1M,1N
33	RES, CARBON 1/4W +5%, 100	942-201-01	3	R16,R27,R29
34	RES, CARBON 1/4W +5%, 1K	942-201-02	15	R1,R2,R4,R5,R7,R8,R10, R11,R13,R28,R33,R34,R40,
35	RES, CARBON 1/4W +5%, 10K	942-201-03	1	R32 R41 R4(
36	RES, CARBON 1/4W +5%, 10M	942-201-06	2	R22,R36
37	RES, CARBON 1/4W +5%, 20K	942-202-03	1	R19
38	RES, CARBON 1/4W +5%, 220	942-202-21	1	R14
39	RES, CARBON 1/4W +5%, 2.2K	942-202-22	1	R24
40	RES, CARBON 1/4W +5%, 220K	942-202-24	2	R21,R25
41	RES, CARBON 1/4W +5%, 27	942-202-70	1	R26
42	RES, CARBON 1/4W +5%, 3.3K	942-203-32	1	R23
43	RES, CARBON 1/4W +5%, 330K	942-203-34	1	R37
44	RES, CARBON 1/4W +5%, 4.7K	942-204-72	1	R17
45	RES, CARBON 1/4W +5%, 470K	942-204-74	1	R15
46	RES, CARBON 1/4W +5%, 680	942-206-81	5	R3,R6,R9,R12,R35
47	RES, CARBON 1/4W +5%, 6.8K	942-206-82	6	R38,R39,R42-R45
48	RES, CARBON 1/4W +5%, 6.8M	942-206-85	1	R20

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, CPU		245-4110-02	B
	MODEL NO. 245	DATE 12-13-83	SHEET 5 OF 6

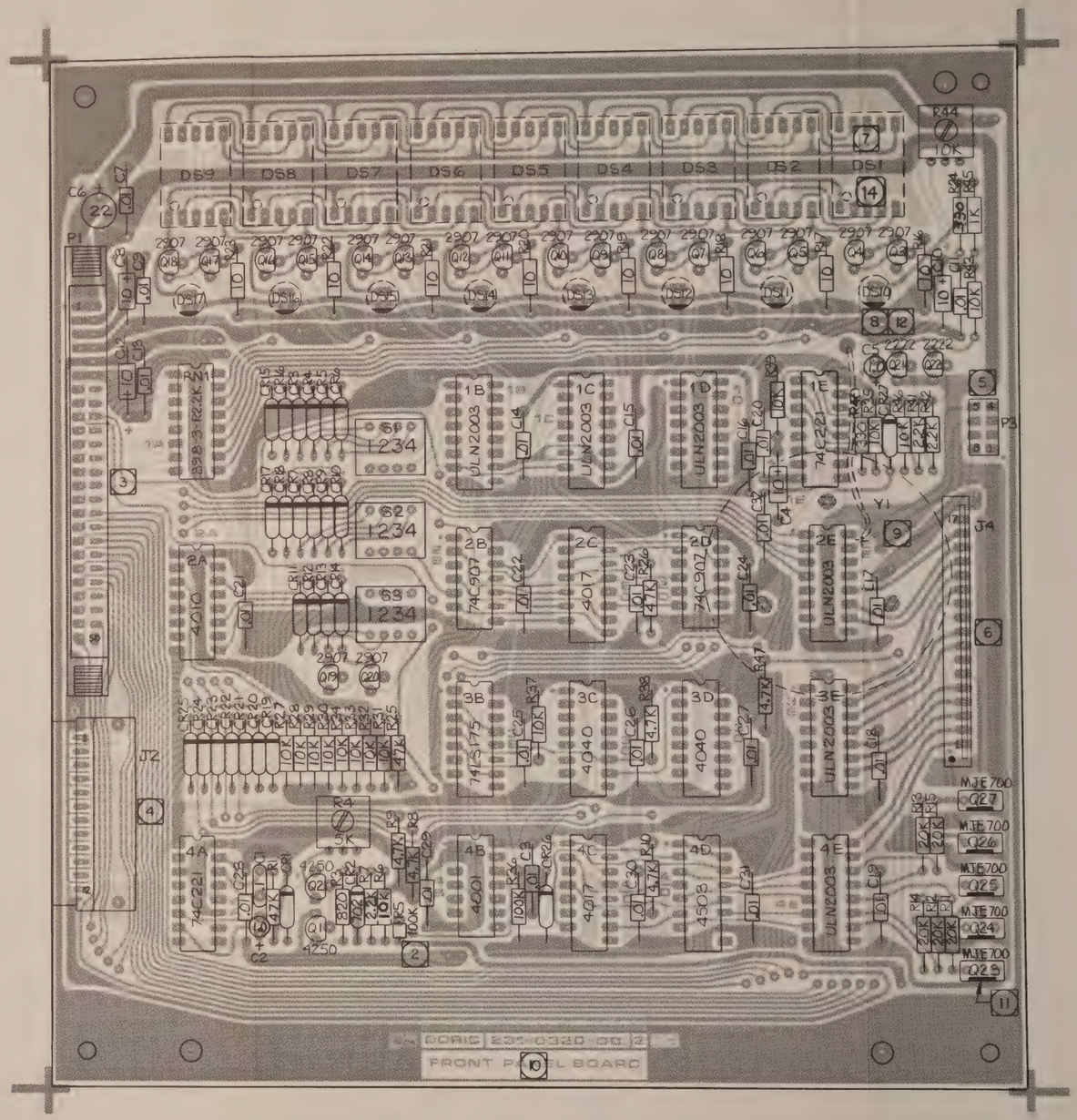
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, NETWK, 6.8K SIP	950-068-01	7	RN1-RN7
50	RES, NETWK, 2.2K SIP	952-022-01	1	RN8
51				
52				
53	CAP, DISC .01 @ 500V	900-021-04	1	C18
54	CAP, AXIAL .01 @ 50V	900-021-07	2	C24,C25
55	CAP, AXIAL .1 @ 50V VARADYNE 1802	900-021-08	39	C6-8,C10-16,C19,C20,C31-C45,C47-49,C51,C52,C54-C60
56	CAP, DISC .001 @ 1KV (5GA)	900-081-03	1	C23
57	CAP, DISC 100pf @ 1KV (5GA)	901-011-01	7	C1-C4,C17,C22,C27
58	CAP, MICA 10pf	915-031-00	1	C28
59	CAP, MICA 15pf	915-031-50	1	C29
60	CAP, TANT, 1 @ 25V (162D)	916-001-25	2	C5,C26
61	CAP, TANT, 3.3 @ 25V (162D)	916-033-25	6	C9,C21,C30,C46,C50,C53
62	CAP, AXIAL .001 @ 50V ±10%	900-021-09	1	C61
63				
64				
65	DIODE, 1N914 (1N4148)	961-091-40	4	CR2,CR3,CR5,CR6
66	DIODE, 8069 DCQ	961-501-02	1	CR1
67	DIODE, ZENER 1N5221B	961-522-12	1	CR4
68				
69				
70	POT, 50K BECKMAN (68X)	960-050-02	1	R18
71				
72	XSTR, 2N2907	962-290-70	1	Q12

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, CPU		245-4110-02	B
	MODEL NO. 245	DATE 12-13-83	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	XSTR, 2N3640	962-364-00	1	Q9
74	XSTR, 2N3646	962-364-60	7	Q1-Q4,Q10,Q11, Q13
75	XSTR, 2N4250	962-425-00	2	Q6,Q7
76	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q5,Q8
77	XTAL, 32.768 KHz	967-005-23	1	Y1
78	SWITCH, DIP, 1 SECTION, FORM A	969-050-09	1	S1
79	CONN, 40 PIN	973-0710-00	1	P2
80	CONN, 50 PIN	973-0710-01	1	P3
81	HEADER, 7 PIN	973-0101-31	1	TP1-TP7
82	BATTERY, 3.6V NICAD	975-100-11	1	BT1
83	HEADER, 3 PIN	973-0101-30	1	TP12-TP14
84	SCREW, PAN HD PHILLIPS, 2-56 X 1/2 LG	980-256-050	2	(P2)
85	SCREW, PAN HD PHILLIPS, 6-32 X 1/2 LG	980-632-050	1	
86	NUT, HEX 2-56	984-100-256	2	(P2)
87	WASHER, FLAT #6	986-100-06	1	
88	WASHER, SPLITLOCK #2	986-200-02	2	(P2)
89	WASHER, SPLITLOCK #6	986-200-06	1	
90	CHASSIS FASTENER, 6-32	991-020-26	1	
91	HEADER, 4 PIN	973-3700-14	1	TP8-TP11
92				
93	SOCKET, IC, 28 PIN	992-010-85	4	(2E,2F,2G,2H)
94				
95	SOCKET, IC, 24 PIN	992-010-35	1	(4D)
96	JUMPER JAX	991-0100-50	1	JMP1



ASSEMBLY-
FRONT PANEL BOARD
231-4320-00E

I.C. POWER DISTRIBUTION TABLE

REFERENCE DESIG	IC TYPE	POWER +5V	GND	+16P	+5VL	PGND	CGND
4C, 4D	4017	16	8	—	—	—	—
1A, 1E	74C221	16	8	—	—	—	—
4A	4503	16	8	—	—	—	—
2E, 3E, 4E	ULN2003	—	—	9	—	8	—
4B	4001	14	7	—	—	—	—
3B	74LS175	16	8	—	—	—	—
3C, 3D	4040	16	8	—	—	—	—
2A	4040	16	8	—	—	—	—
1B, 1C 1D	ULN2003	—	—	—	9	—	8
2B, 2D	74C907	14	7	—	—	—	—

DESIGNATORS

	LAST USED	DO NOT USE
CAPACITORS	C32	
RESISTORS	R47	R2
DIODES	CR27	
TRANSISTORS	Q27	
SWITCHES	S3	
RES NET WK	RN1	
CONNECTORS	P3	
[illegible]	[illegible]	
[illegible]	Y1	
DISPLAYS	DS17	

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIODES ARE 1N914 OR 1N4148.
2. RESISTANCE VALUES ARE IN OHMS.
3. CAPACITANCE VALUES ARE IN MICRO-FARADS.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		-	LIMITED USAGE RELEASE	[illegible]	[illegible]	[illegible]
		/ 1	LIMITED USAGE RELEASE	[illegible]	9/24/82	[illegible]
		A5	REVISED PER E.O. 2-10196	[illegible]	9/2/82	[illegible]
		B	PRODUCTION RELEASE PER E.O. 2-10403	[illegible]	[illegible]	[illegible]
		C	REVISED PER E.O. 2-10486	[illegible]	11-26-82	[illegible]
		D	REVISED PER E.O.2-10572	[illegible]	12/21/82	[illegible]
		E	ADD BARS TO SIGNAL NAME	[illegible]	2-11	[illegible]
		F	REVISED PER E.O.2-11139	[illegible]	2/8/83	[illegible]

PRINTER TIMMERS

THERMAL PRINTER ASSY NO. 231-4260-00

RIGHTHAND PRINT DOT SELECT

LEFTHAND PRINT DOT SELECT

THERMAL PRINTHEAD (995-100-07)

PRINT COLUMNS

RIGHTHAND PRINT COLUMN

COLUMN SELECTS 1 THRU 12

LEFTHAND PRINT COLUMN

PRINTER MOTOR

BURN START

DOTSTEP

DOT CLOCK

BURN

BURN STOP/ BURN

SEGMENT STEPPER DRIVER

ULN2003

COLUMN DRIVER

STEP A

STEP B

STEP C

STEP D

COL 1

COL 2

COL 3

COL 4

COL 5

ASSEMBLY NO	230-4320-00
SUPERSEDES	231-6320-00 C
DES/ENG	[illegible]
DRAWN	RENE HERROM 3-80
CHECK	[illegible] 5-30-80
APPR.	[illegible]

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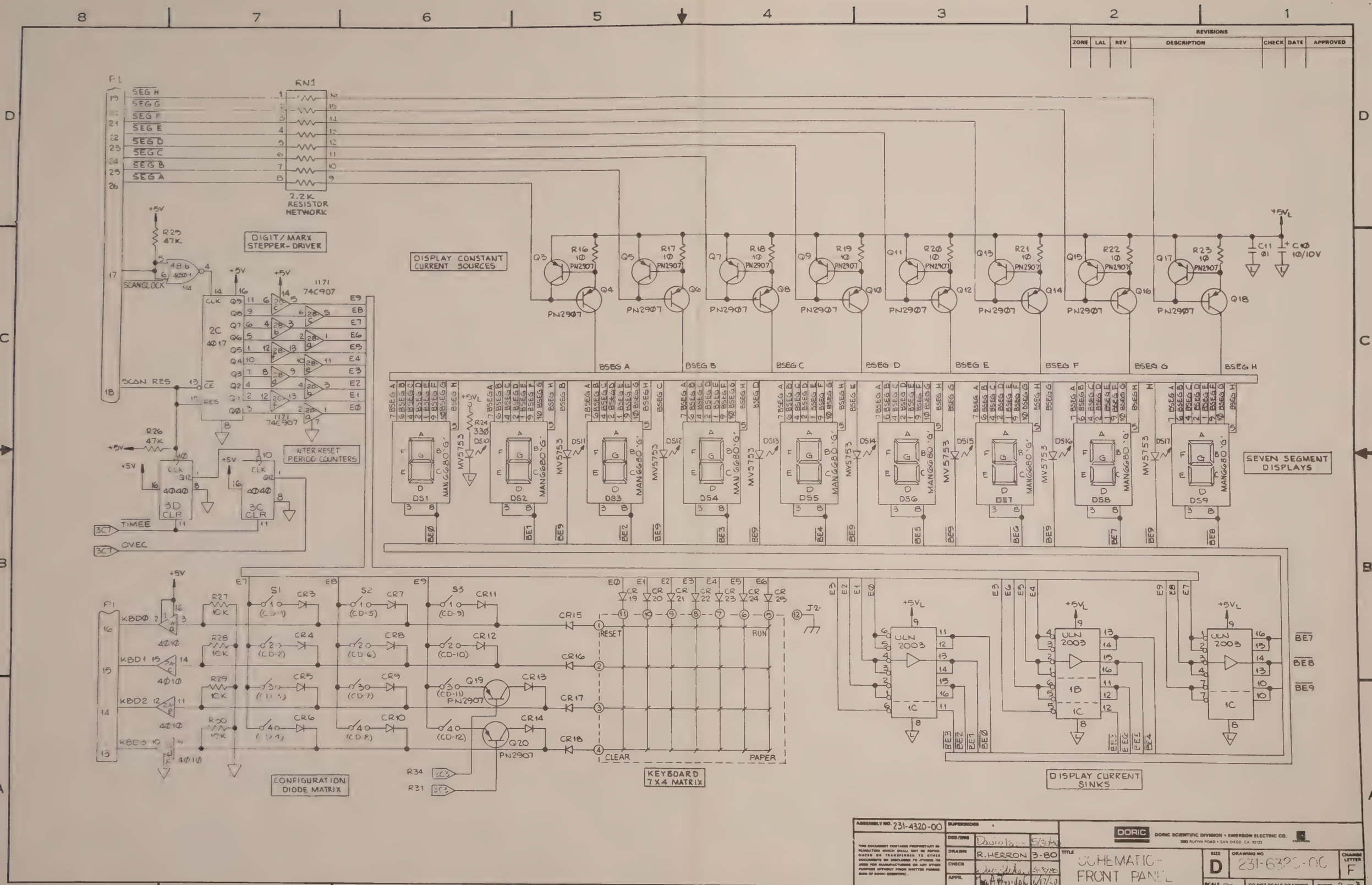
DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

TITLE: SCHEMATIC - FRONT PANEL

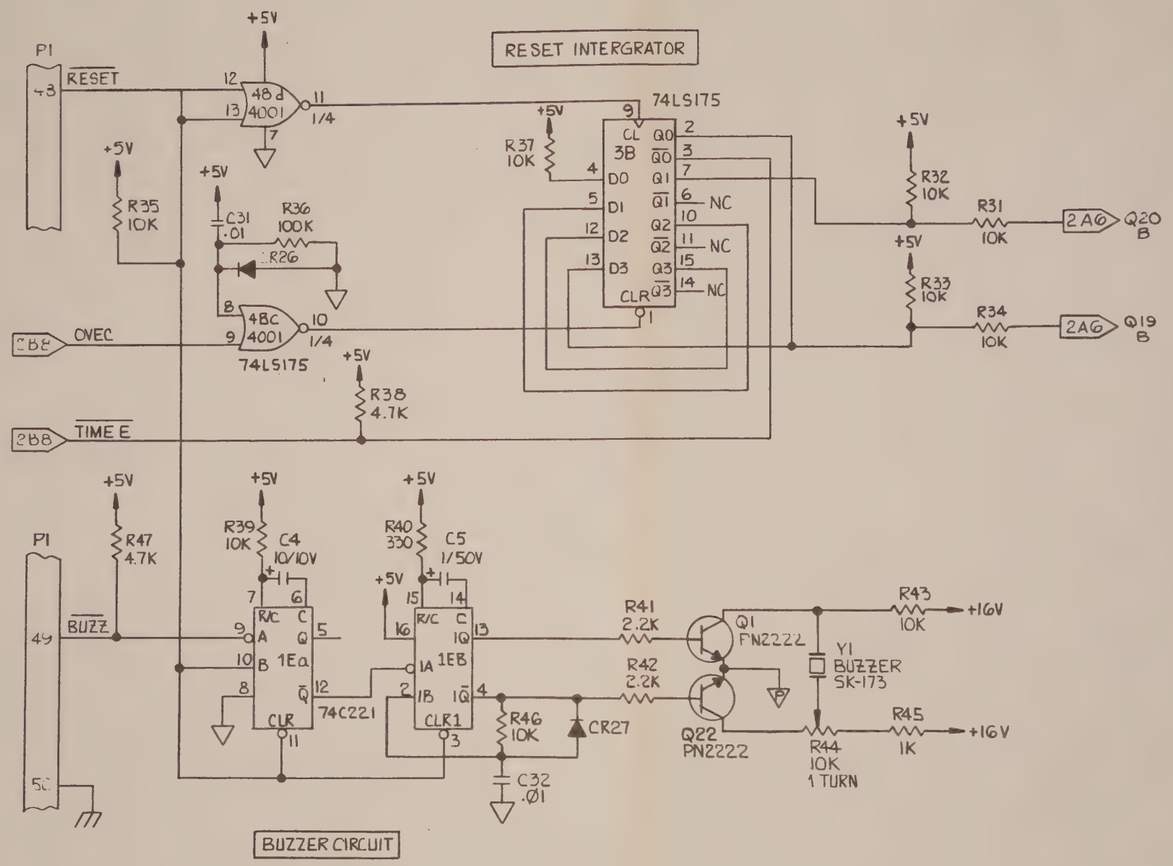
SIZE: D | DRAWING NO.: 231-6320-00 | CHANGE LETTER: F

SCALE: —— | DO NOT SCALE DRAWING | SHEET 1 OF 3



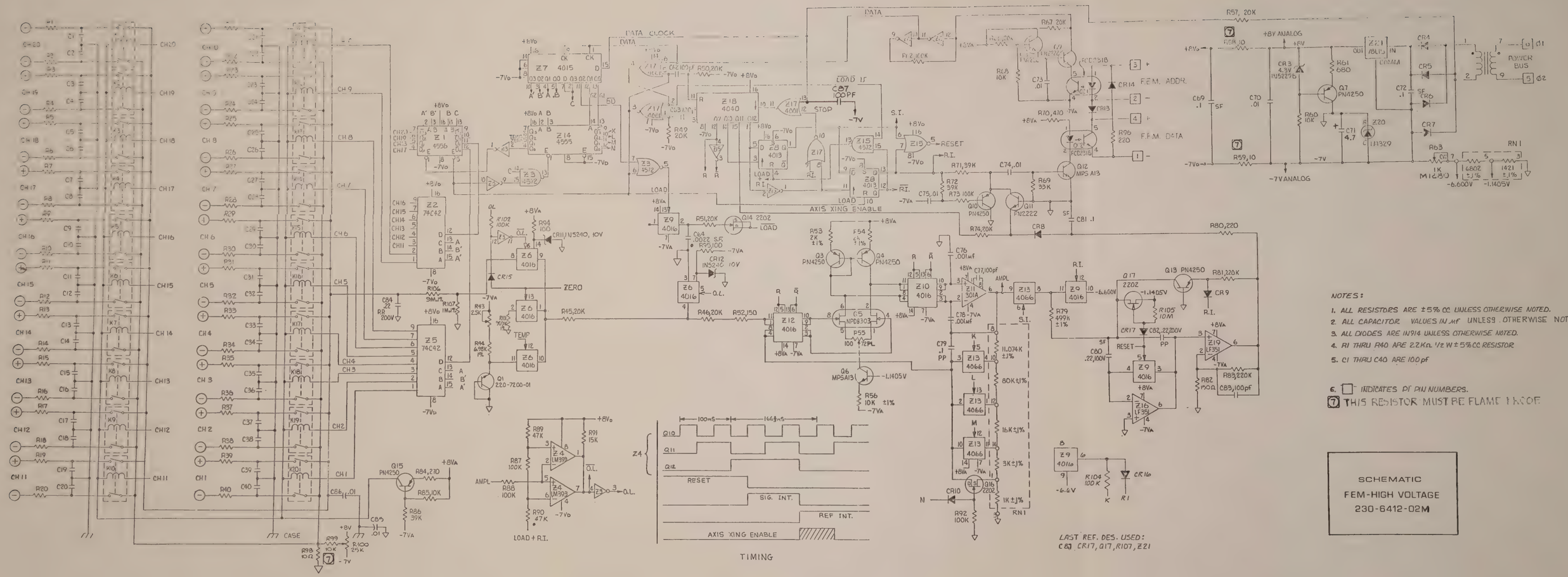
REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
RN1
2.2K RESISTOR NETWORK
DIGIT/MARX STEPPER-DRIVER
DISPLAY CONSTANT CURRENT SOURCES
SEVEN SEGMENT DISPLAYS
INTER RESET PERIOD COUNTERS
CONFIGURATION DIODE MATRIX
KEYBOARD 7X4 MATRIX
DISPLAY CURRENT SINKS
SCAN CLOCK
SCAN RES
TIMEE
OVEC
RESET
RUN
CLEAR
PAPER
ASSEMBLY NO. 231-4320-00
SUPERSEDES
DRAWN R. HERRON 3-80
DORIC
DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
TITLE SCHEMATIC - FRONT PANEL
SIZE D
DRAWING NO 231-6320-00
CHANGE LETTER F
SCALE ~
DO NOT SCALE DRAWING
SHEET 2 OF 3

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



BUZZER CIRCUIT

SIZE	CODE IDENT. NO.	DRAWING NO.	CHANGE LETTER
D		231-6320-00	F
SCALE ——	DO NOT SCALE DRAWING	SHEET 3 OF 3	



NOTES:

1. ALL RESISTORS ARE ±5% CC UNLESS OTHERWISE NOTED.
2. ALL CAPACITOR VALUES IN mf UNLESS OTHERWISE NOTED.
3. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED.
4. R1 THRU R40 ARE 2.2Kn. 1/2 W ± 5% CC RESISTOR
5. C1 THRU C40 ARE 100 pf
6. □ INDICATES PT PIN NUMBERS.
7. THIS RESISTOR MUST BE FLAME PROOF

SCHEMATIC
FEM-HIGH VOLTAGE
230-6412-02M

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
PCB ASSEMBLY, HIGH VOLTAGE FEM	MODEL NO. 235	230-4412-02	V
		DATE 3-17-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB REED FEM	230-2410-02	1	
2	SCHEMATIC	230-6412-02	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
7	IC, 4001 4-2IN NOR CMOS(MO)	965-587-01	1	Z17
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z7
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	Z8
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	2	Z2,Z5
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z18
13	IC, 4556 DUAL 10F4 DEC(MO,FC,NL	965-587-48	1	Z1
14	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
15	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z11
16	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z16,Z19
17	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z3,Z15
18	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z20
19	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z21
20				
21				
22				
23				
24				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE FEM	MODEL NO. 235	230-4412-02	V
		DATE 3-17-89	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C, 499K	920-449-93	1	R79
26	RES, FILM RN55D 1% 10K	924-310-02	1	R56
27	RES, FILM RN55C 2K	924-420-01	2	R53,R54
28	RES, FILM RN55C 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W +-5%, 10	940-001-00	3	R58,R59,R98
30	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R94,R95
31				
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	4	R60,R68,R85,R99
33	RES, CARBON 1/4W ± 5%, 100K	942-201-04	7	R62,R73,R87-88 R92,R102,R104
34	RES, CARBON 1/4W ± 5%, 10M	942-201-06	1	,R105
35				
36	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
37	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R91
38	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
39	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R96
40	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
41	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R84
42	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69
43				
44	RES, CARBON 1/4W ± 5%, 39K	942-203-93	3	R71-72,R86
45	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
46				
47	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R89,R90
48	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE FEM	MODEL NO. 235	230-4412-02	V
		DATE 3-17-80	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	40	R1-R40
50	RES, FILM RN55C, 909K 1%	924-490-93	1	R101
51	RES, 0.1%, 9M (CADDOCK MK132)	922-590-04	1	R106
52	RES, 0.1%, 1M (CADDOCK MK632)	922-510-04	1	R107
53				
54	CAP, TANT 4.7 @ 35V (1960)	916-470-35	1	C71
55	CAP, DISC .01/500V (5GA)	900-021-04	6	C70 ,C73-75, C85,C86
56	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
57	CAP, DISC, 100 PF @ 1 KV (5GA)	901-011-01	45	C1-40,C62-63, C77,C83,C87
58	CAP, PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
59	CAP, PLP,.22/200V,IMB(GA2C224K)	917-022-20	2	C82,C84
60				
61	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C69,C72,C81
62	CAP, SF, .0022/250V, SMS(B32570)	918-002-25	1	C64
63	CAP,SF, .22/100V, SMS(B32570)	918-022-10	1	C80
64				
65				
66				
67				
68				
69	DIODE, 1N914 (1N4148)(RD,FC,TI	961-091-40	12	CR4-10,CR13-17
70	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
71				
72	DIODE, IN5240, 10V	961-524-00	2	CR11,CR12

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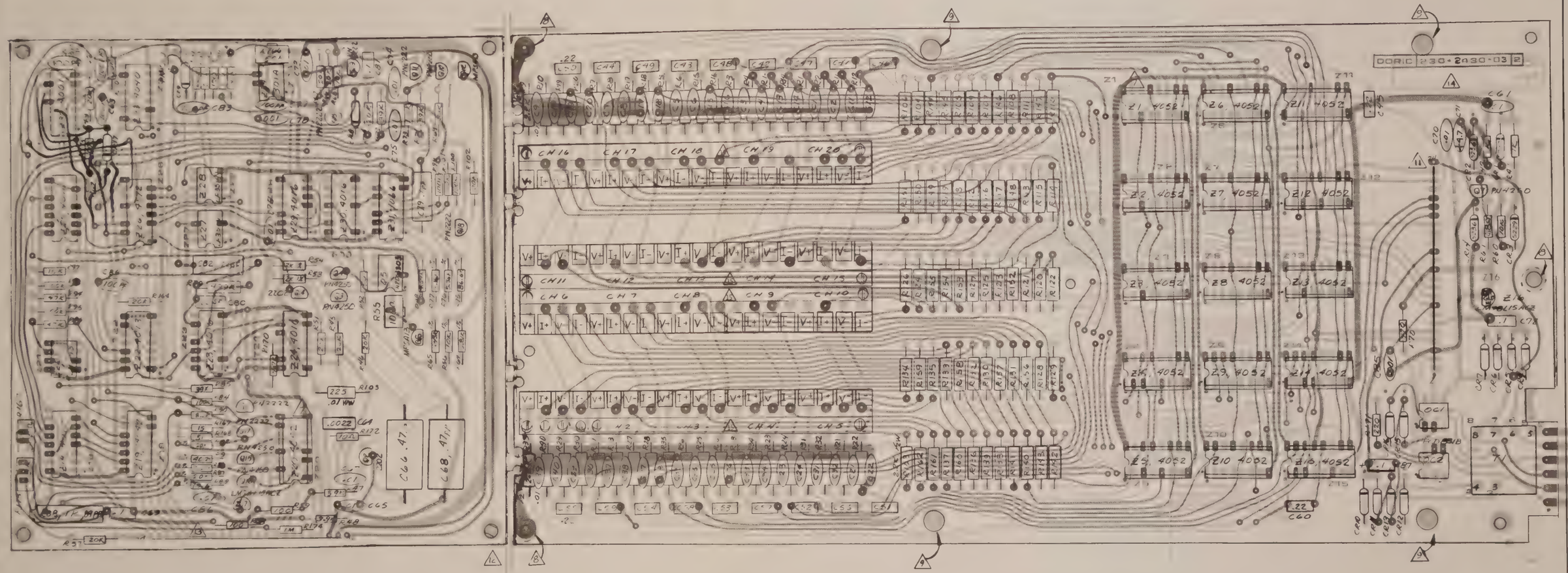
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE FEM	MODEL NO. 235	230-4412-02	V
		DATE 3-17-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
78	GRADED 4016	000-7700-00	4	Z6,Z9,Z10,Z12
79	RELAY, REED LOW THERMAL	000-8043-00	20	K1-K20
80	FET, 2202 (NJ,LO-LK,GP)	100-722-02	3	Q14,Q16,Q17
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
83	POT, 100 CERMET (72PL)	960-015-19	1	R55
84	POT, 25K MT2X253	960-015-15	2	R100, R43
85	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
86	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	6	Q3-4,Q7,Q10-11, Q15
87	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Q5
88	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
89	OPTO, FCD8316 (FC)	965-570-03	2	OC1,OC2
90	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
91	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
92	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	6	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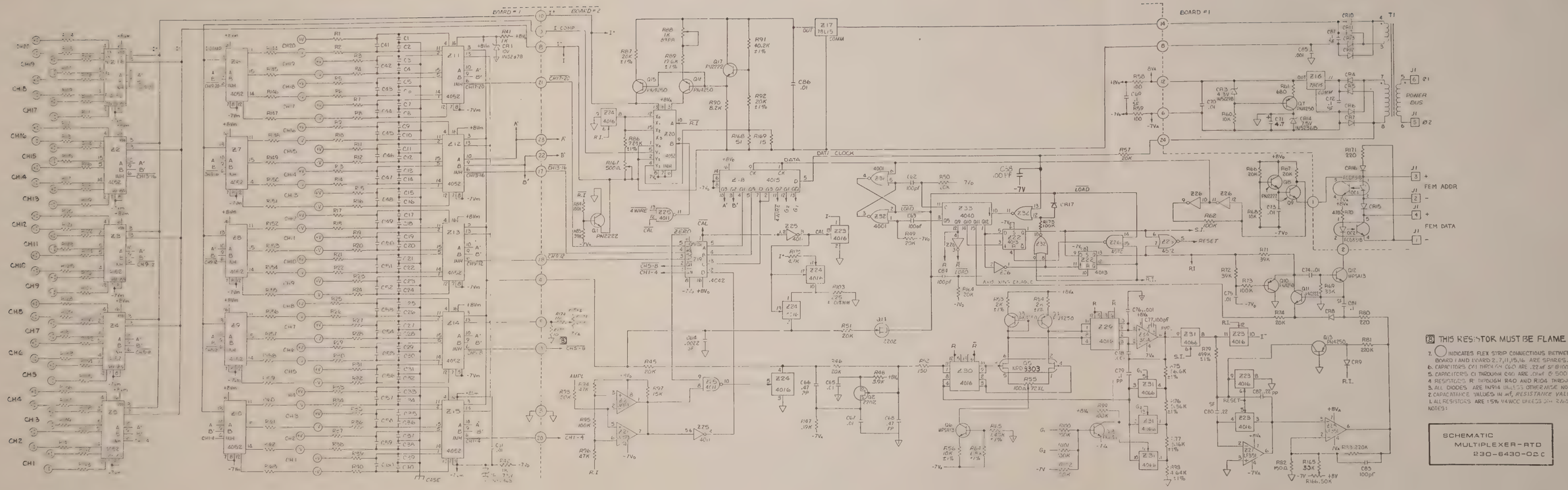
ASSEMBLY
RTD FEM
230-4430-02C



8. THIS RESISTOR MUST BE FLAME PROOF.

7. ○ INDICATES FLEX STRIP CONNECTIONS BETWEEN BOARD I AND BOARD 2. 7, 11, 15, 16 ARE SPARES.
6. CAPACITORS C61 THRU C64 C60 ARE .22 uF @ 100V.
5. CAPACITORS C1 THROUGH C60 ARE .01uF @ 500V.
4. RESISTORS R THROUGH R40 AND R104 THROUGH R163 ARE ½W 5% CC.
3. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED
2. CAPACITANCE VALUES IN uF, RESISTANCE VALUES IN Ω.
1. ALL RESISTORS ARE 1% ¼WCC UNLESS OTH ERWISE NOTED.

NOTES:

SCHEMATIC
MULTIPLEXER-RTD
230-6430-02C

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	DATE 3-18-80	SHEET 3 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, RTD MULTIPLEXER	230-2430-03	1	
2	SCHEMATIC	230-6430-02	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z21
7	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z32
8	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z25
9	IC, 4015 DUAL SE CMOS (MO)	965-587-03	1	Z18
10	IC, GRADED 4066	000-8130-00	1	Z31
11	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z22
12	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z19
13	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z33
14	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z34
15	IC, LF351N FET OP AMP (NL)	965-616-01	2	Z27,Z28
16	IC, 4572 INV, NOR, NAND CMOS(MO)	965-618-00	1	Z26
17	IC, LM8L15ACZ 15V REG92(NL)	965-637-00	2	Z16,Z17
18				
19				
20				
21				
22				
23	RES, FILM RN60C, 499K	920-449-93	1	R79
24	RES, FILM RN55D 1% 10K	924-310-02	1	R56

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	DATE 3-18-80	SHEET 4 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D 1.43K	924-314-30	1	R65
26	RES, FILM RN55D 19.6K	924-319-62	1	R89
27	RES, FILM RN55D 1% 20K	924-320-02	2	R87,R92
28	RES, FILM RN55D 3.16K	924-331-61	1	R77
29	RES, FILM RN55D 40.2K	924-340-22	1	R91
30	RES, FILM RN55D 4.64K	924-346-41	1	R98
31	RES, FILM RN55D 5.36K	924-353-62	1	R76
32	RES, FILM RN55D 6.81K	924-368-12	1	R64
33	RES, FILM RN55D 7.23K	924-372-32	1	R86
34	RES, FILM RN55D 86.6K	924-386-62	1	R75
35	RES, FILM RN55C 2K	924-420-01	2	R53,R54
36	RES, FILM .01% W/W 225 (ElTYPE27)	937-201-28	1	R103
37	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R58,R59
38	RES, CARBON 1/4W ± 5%, 1K	942-201-02	2	R41,R42
39	RES, CARBON 1/4W ± 5%, 10K	942-201-03	2	R60,R68
40	RES, CARBON 1/4W ± 5%, 100K	942-201-04	10	R62,R73,R84,R93, R95,R99-102,R175
41	RES, CARBON 1/4W ± 5%, 15	942-201-50	1	R169
42	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
43	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R97
44	RES, CARBON 1/4W ± 5%, 30K	942-203-03	1	R165
45	RES, CARBON 1/4W ± 5%, 20K	942-202-03	10	R45-46,R49-51,57 R66-67,R74,R164
46	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R171
47	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
48	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	230-4430-02	C
	DATE 3-18-80	SHEET 5 OF 7	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
50	RES, CARBON 1/4W ± 5%, 39K	942-203-93	4	R47,R71,R72,R85
51	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
52	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R170
53	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R94,R96
54	RES, CARBON 1/4W ± 5%, 51	942-205-10	1	R168
55	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61
56	RES, CARBON 1/4W ± 5%, 8.2K	942-208-22	1	R90
57	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	100	R1-40,R104-163
58	RES, CARBON 1/4W ± 5%, 1M	942-201-05	1	R174
59	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	1	R172
60				
61				
62	CAP, TANT, 4.7 @ 35V (1960)	916-470-35	1	C71
63	CAP, DISC, .01 @ 500V (5GA)	900-021-04	48	C1-40,70,73-75, 61,65,67,86
64	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	3	C76,C78,C85
65	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	6	C62,C63,C77,C83, C84,C88
66	CAP,PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
67	CAP,PLP,.22/200V,IMB(GA2C224K)	917-022-20	1	C82
68	CAP,PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
69	CAP, SF, .1/100V, SMS(B32570)	918-001-10	4	C72,C69,C81,C87
70	CAP, SF, .0022/250V,SMS(B32570)	918-002-25	1	C64
71	CAP, SF, .22/100V, SMS(B32570)	918-022-10	21	C41-60,C80
72				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	230-4430-02	C
	DATE 3-18-80	SHEET 6 OF 7	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	13	CR4-13,CR15-17
78	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
79	DIODE, 1N5236B (7.5V)	961-523-62	2	CR2,CR14
80	DIODE, 1N5237B 8.2V (MO)	961-523-72	1	CR1
81				
82				
83				
84				
85				
86	GRADED 4016	000-7700-00	4	Z23-24,Z29-30
87	SELECTED 4052 CMOS MULTI	000-8051-00	16	Z1-15,Z20
88	FET, 2202 (NJ,L)-LK,GP)	100-722-02	2	Q2,Q14
89	XFMR. RTD INTERFACE	230-7060-00	1	T1
90	POT, 1K CERMET (89PR)	960-011-02	1	R88
91	POT, 100 CERMET (72XL)	960-011-17	1	R55
92	POT, 500 CERMET (72XL)	960-015-07	1	R167
93	POT, 50K CERMET (72XL)	960-015-08	1	R166
94	POT, 25K CERMET (72XL)	960-015-10	1	R173
95	XSTR, PN2222 (NPNA92)(NA)	962-222-20	6	Q1,Q8,Q9,Q11, Q17,Q18
96	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	7	Q3-4,Q10,Q13, Q7,Q15-16

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	230-4430-02	C
	DATE 3-18-80	SHEET 7 OF 7	

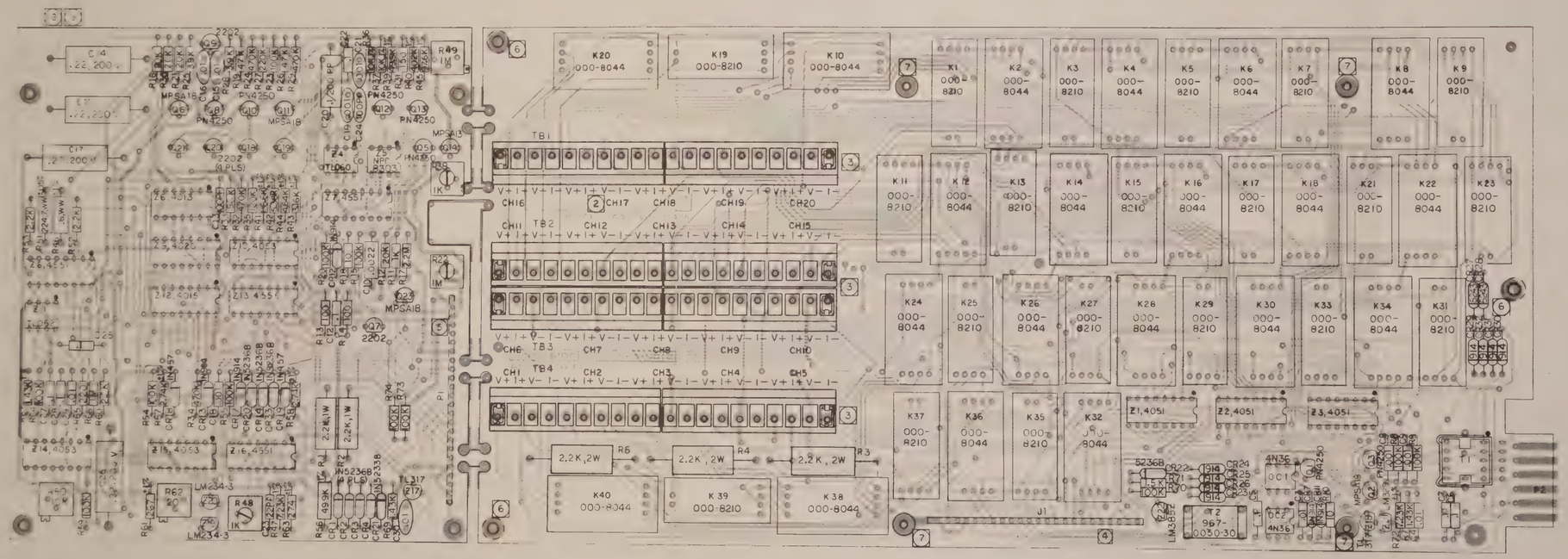
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Q5
98	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
99	OPTO, FCD831B (FC)	965-570-03	2	OC1,OC2
100	T.S 20P ELCTVT 8145 251352053	973-010-55	4	
101	STDF, 5/8X440 A2(L6911-10-2A)	991-020-85	4	
102	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	3	
103	IC SOCKET, 16DIP LP (516AG11D)	992-010-10	16	
104	FLAT CBL, 3(ANSLEY FSN-23A-24)	993-100-07	1	
105	WASHER, SPLITLOCK 4	986-200-04	4	
106	WASHER, FLAT 4	986-100-04	4	
107	SCREW, PAN HD. PHILLIPS, 4-40 X 5/16"	980-440-031	4	
108	DISS-O-PAD .025 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	12	

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A1	LTD USAGE REL PER E.O. 2-11377	RB	5-1-84	[illegible]
		A2	REVISED PER E.O. 2-11448	[illegible]	[illegible]	[illegible]
		B	PRODUCTION REL PER E.O. 2-11484	[illegible]	[illegible]	[illegible]

7. INSTALL 1/2" LONG STANDOFF (ITEM 104) ON NEAR SIDE (COMP SIDE).
8. DELETED
9. COMPONENTS TO BE 9/32" HIGH MAXIMUM (TOP BD).
10. RESISTANCE IN OHMS ±5%, 1/4 WATT.
11. CAPACITANCE IN MICROFARADS.
12. ALL COMP LEADS ON THIS BOARD (TOP BD) TO BE TRIMMED TO .031 MAXIMUM LENGTH.

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED PER DORIC SPEC 000-1003.
2. RUBBER STAMP ASSEMBLY NUMBER AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR SIDE (SLDR SIDE) OF BOARD.
3. INSTALL TERMINAL STRIP (ITEM 119), 8 PLACES.
4. INSTALL CONN 24 PIN FEM (ITEM 106) NEAR SIDE (COMP. SIDE).
5. INSTALL CONN 24 PIN MALE (ITEM 107) FARSIDE (SLDR SIDE).
6. INSTALL 1/8" LONG SPACER (ITEM 105) ON FAR SIDE (SLDR SIDE).



HOLE TOLERANCES	NOTES UNLESS SPECIFIED	DRAWN	CHECK	APPR
.000-.200 DIA +.004-.002 .201-.500 DIA +.005-.002 .501-1.00 DIA +.010-.005	1. TOLERANCES .XX ± .03 DIMENSIONED ANGLES .XXX ± .010 ± ½° 2. BREAK ALL SHARP EDGES .010 APPROX 3. MACH SURFACES J 4. ALL DIM IN INCHES 5. ALL TRUE POSITION TOLERANCES APPLY AT MMC	[illegible]	[illegible]	[illegible]

SUPERSEDES

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC

USED ON: 235

NEXT ASSY: 231-5585-XX

MATERIAL

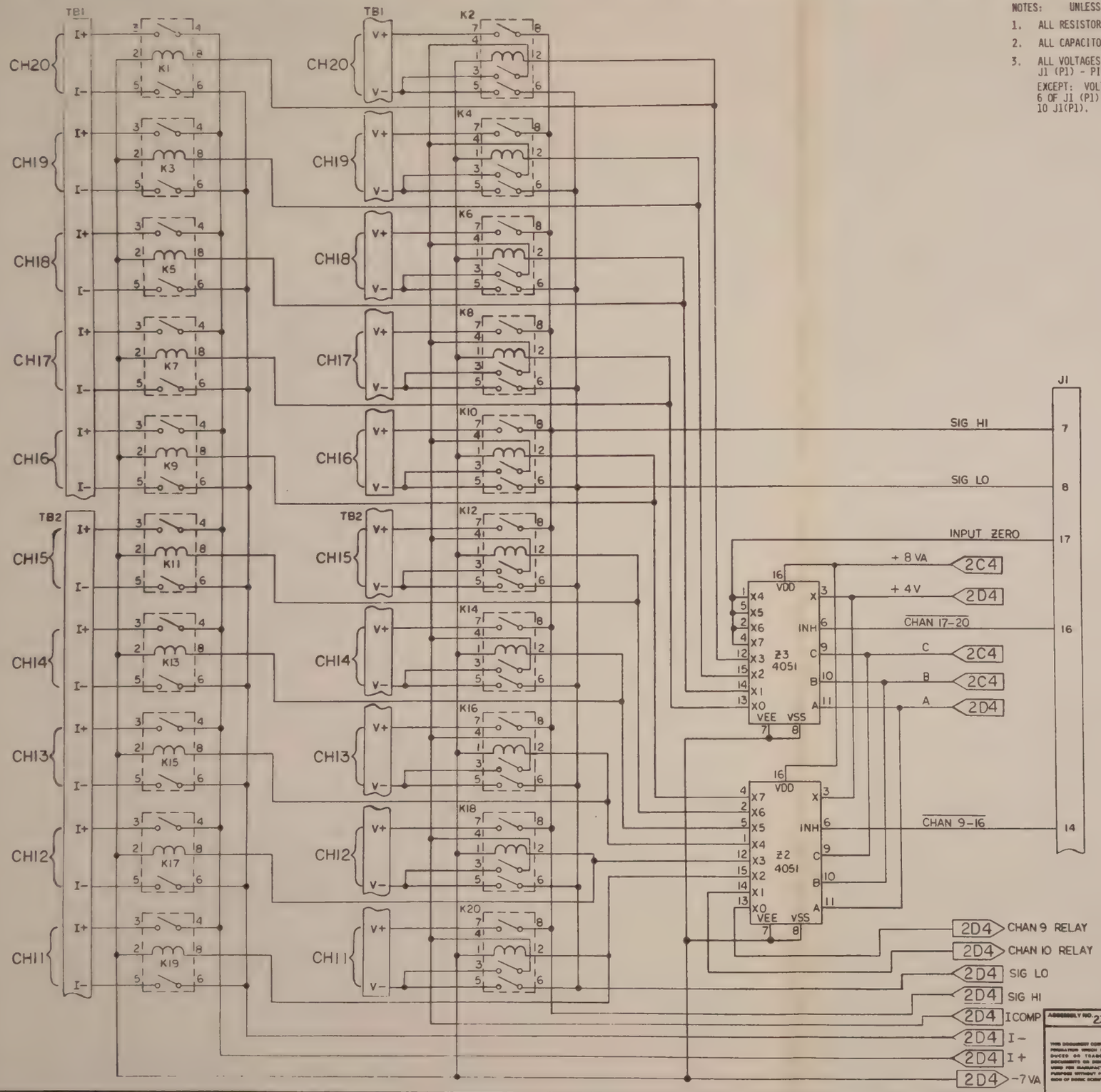
FINISH

DORIC — DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3800 RUFFIN ROAD • SAN DIEGO, CA 92123

TITLE: ASSEMBLY, PCB, REED RTD FEM

SIZE | CODE IDENT. NO. | DRAWING NO. 231-4585-00 | CHANGE LETTER B

SCALE 2/1 | DO NOT SCALE DRAWING | SHEET 1 OF 7



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±5%, C.C. 1/4W.
2. ALL CAPACITORS VALUES ARE IN MICROFARADS.
3. ALL VOLTAGES REFERENCED TO ANALOG GROUND (⏚) J1 (P1) - PIN 5
   EXCEPT: VOLTAGES AT PINS 3, 4 AND PIN 6 OF J1 (P1) ARE REFERENCED TO PIN 10 J1(P1).

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A1	LTD USAGE REL PER E.O. 2-11377			
		A2	REVISED PER E.O. 2-11448			
		B	PRODUCTION REL PER E.O. 2-11484			
		C	REVISED PER E.O. 2-11573	SD		

REFERENCE DESIGNATOR CHART		
REF. DES	LAST USED	UNUSED
RESISTORS	R74	
CAPACITORS	C29	C1, C2
TRANSISTORS	Q23	Q4, Q15-Q17 Q22
I.C.'S	Z22	
DIODES	CR33	CR5, CR6, CR8
RELAYS	K40	
OPTO-COUPLER	OC2	
TRANSFORMERS	T2	
TERMINAL BLOCKS	TB4	
CONNECTORS	J2	
CONNECTORS	P1	

ASSEMBLY NO. 231-4585-XX

SUPERSEDES

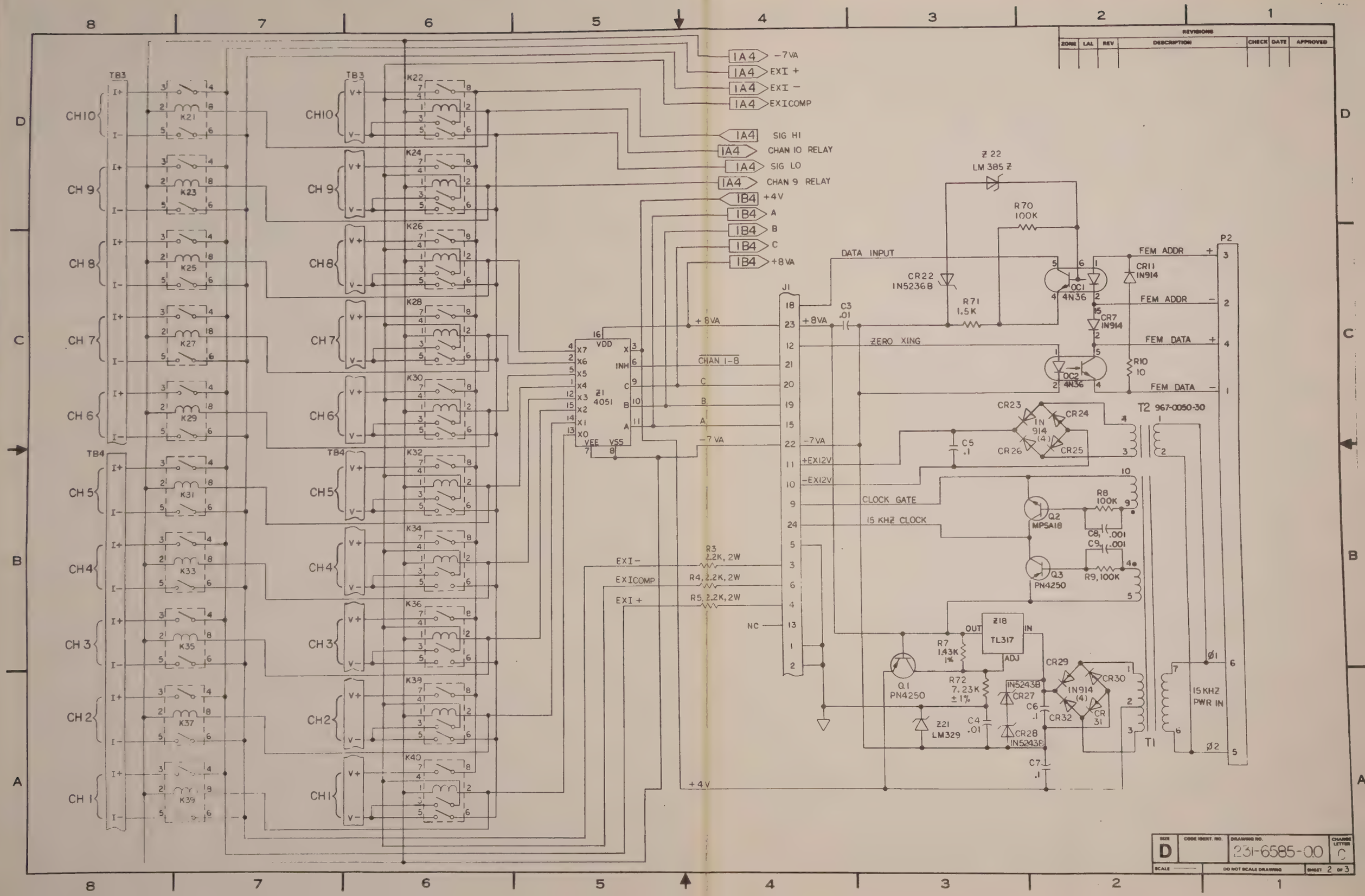
DES/ENG 5-16-83
DRAWN M. FRANK 7-12-83
CHECK
APPR.

DORIC — DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO

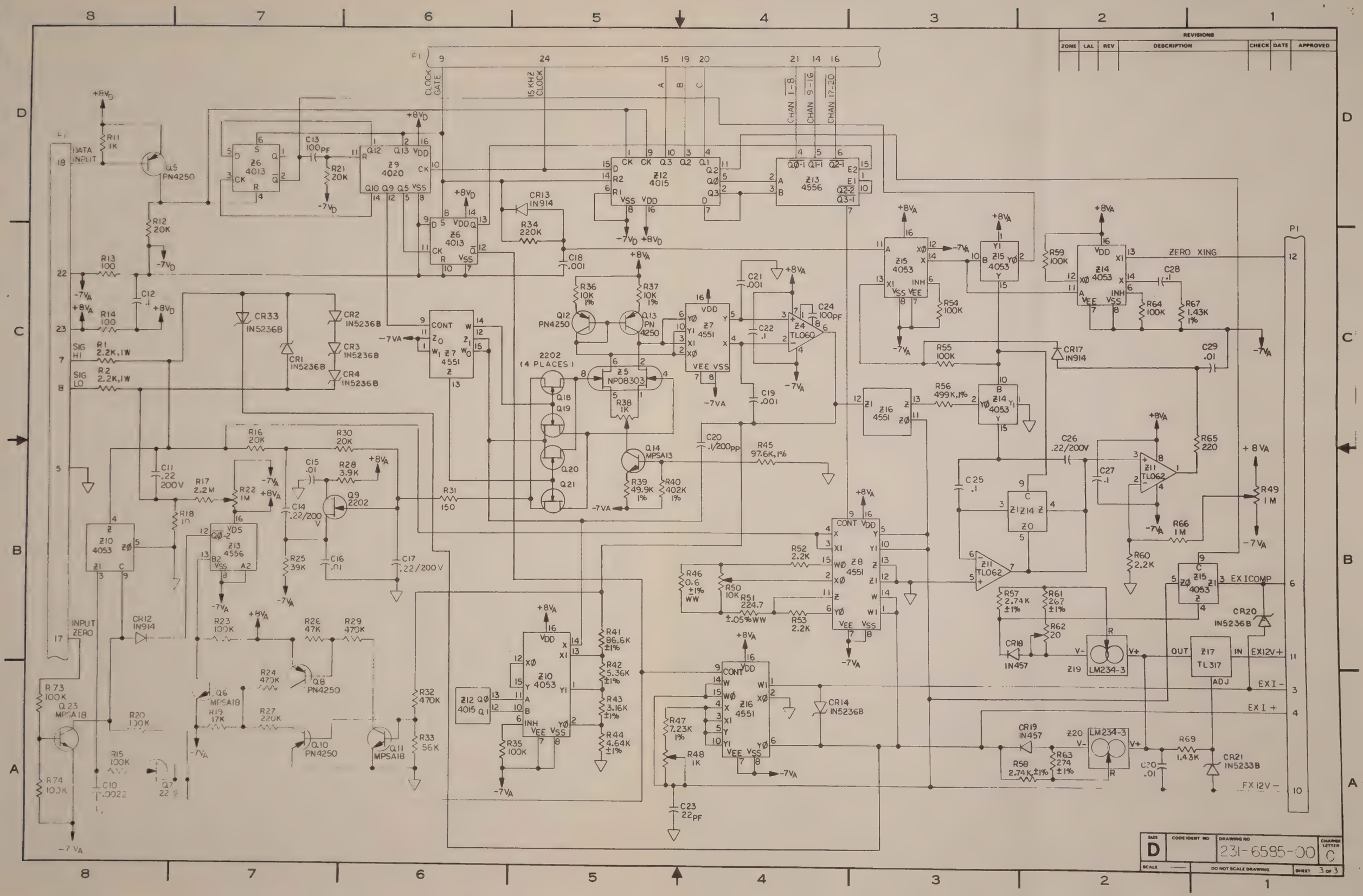
TITLE SCHEMATIC, REED RTD FEM

SIZE D — DRAWING NO. 231-6585-00 — CHANGE LETTER C

SCALE — DO NOT SCALE DRAWING — SHEET 1 OF 3



REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
TB3
TB4
CH10
CH 9
CH 8
CH 7
CH 6
CH 5
CH 4
CH 3
CH 2
CH 1
K21
K23
K25
K27
K29
K31
K33
K35
K37
K39
K22
K24
K26
K28
K30
K32
K34
K36
K38
K40
1A4 -7VA
1A4 EXI +
1A4 EXI -
1A4 EXICOMP
1A4 SIG HI
1A4 CHAN 10 RELAY
1A4 SIG LO
1A4 CHAN 9 RELAY
1B4 +4V
1B4 A
1B4 B
1B4 C
1B4 +8VA
Z1 4051
VDD
INH
VEE
VSS
CHAN 1-8
+8VA
-7 VA
EXI-
EXICOMP
EXI +
R3 2.2K, 2W
R4, 2.2K, 2W
R5, 2.2K, 2W
NC
J1
+8VA
-7VA
+EX12V
-EX12V
+4V
DATA INPUT
ZERO XING
CLOCK GATE
15 KHZ CLOCK
C3 .01
Z 22 LM 385 Z
R70 100K
CR22 1N5236B
R71 1.5K
OC1 4N36
OC2 4N36
CR11 1N914
CR7 1N914
R10 10
FEM ADDR
FEM ADDR
FEM DATA
FEM DATA
P2
CR23
CR24
CR25
CR26
1N 914 (4)
C5 .1
T2 967-0050-30
R8 100K
Q2 MPSA18
C8, .001
C9, .001
Q3 PN4250
R9, 100K
Z18 TL317
OUT
IN
ADJ
R7 1.43K 1%
R72 7.23K ±1%
Q1 PN4250
Z21 LM329
C4 .01
1N5243B
CR27
CR28
1N5243B
C6 .1
C7 .1
CR29
CR30
CR31
CR32
1N914 (4)
T1
Ø1
Ø2
15 KHZ PWR IN
SIZE
D
CODE IDENT. NO.
DRAWING NO.
231-6585-00
CHANGE LETTER
C
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 3



REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
P1
CLOCK GATE
15 KHZ CLOCK
CHAN 1-8
CHAN 9-16
CHAN 17-20
DATA INPUT
INPUT ZERO
SIG HI
SIG LO
ZERO XING
EXICOMP
EX12V+
EXI-
EXI+
EX12V-
Z6 4013
Z9 4020
Z12 4015
Z13 4556
Z15 4053
Z14 4053
Z7 4551
Z4 TL060
Z5 NPD8303
Z16 4551
Z8 4551
Z10 4053
Z11 TL062
Z17 TL317
Z19 LM234-3
Z20 LM234-3
Q5 PN4250
Q12 PN4250
Q13 PN 4250
Q14 MPSA13
Q9 2202
Q23 MPSA18
Q6 MPSA18
Q8 PN4250
Q10 PN4250
Q11 MPSA18
Q7 22 %
2202 (4 PLACES)
CR33 IN5236B
CR1 IN5236B
CR2 IN5236B
CR3 IN5236B
CR4 IN5236B
CR13 IN914
CR12 IN914
CR17 IN914
CR18 IN457
CR19 IN457
CR14 IN5236B
CR20 IN5236B
CR21 IN5233B
+8VD
-7VD
+8VA
-7VA
SIZE D
CODE IDENT NO
DRAWING NO 231-6585-00
CHANGE LETTER C
SCALE
DO NOT SCALE DRAWING
SHEET 3 OF 3

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
ASSEMBLY, PCB, REED RTD FEM	ML	231-4585-00	C
	MODEL NO. 235	DATE 7-7-83	SHEET 3 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, REED RTD FEM	231-2585-00	1	
2	SCHEMATIC, REED RTD FEM	231-6585-00	1	
3	TEST SPEC			
4				
5	IC, LM385Z	961-385-00	1	Z22
6	IC, 4051 8 CHANNEL MUX, SEL	000-8190-00	3	Z1,Z2,Z3
7	IC, 4053 3-2 CHANNEL MUX	965-5870-81	3	Z10,Z14,Z15
8	IC, 4551 4-2 CHANNEL MUX	965-5870-82	3	Z7,Z8,Z16
9	IC, 4015 DUAL SE CMOS	965-587-03	1	Z12
10	IC, 4556 DUAL 1 OF 4 DEC	965-587-48	1	Z13
11	IC, 4013 DUAL D FF CMOS	965-587-23	1	Z6
12	IC, 4020 14 BIT BIN CTR	965-5870-84	1	Z9
13	IC, TL060CP OP AMP	965-646-00	1	Z4
14	IC, TL062CP DUAL OP AMP	965-6170-03	1	Z11
15	IC, LM329BZ 20 PPM REF	965-636-00	1	Z21
16	IC, TL317LP VREG (TI)	965-645-00	2	Z17,Z18
17	IC, REF LM 234-3 (NS)	965-6360-01	2	Z19,Z20
18	RES, CARBON 1/4W ±5%, 2.2K	942-202-22	3	R52,R53,R60
19	RES, FILM RN55C ±1%, 274	924-4274-00	1	R63
20	RES, FILM RN55D ±1%, 1.43K	924-314-30	3	R7,R67,R69
21				
22				
23				
24	RES, FILM RN55D ±1%, 3.16K	924-331-61	1	R43

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, REED RTD FEM	MODEL NO. 235	DATE 7-7-83	SHEET 4 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D ±1%, 4.64K	924-346-41	1	R44
26	RES, FILM RN55D ±1%, 49.9K	924-3499-10	1	R39
27	RES, FILM RN60C ±1%, 499K	920-449-93	1	R56
28	RES, FILM RN55D ±1%, 402K	924-340-23	1	R40
29	RES, FILM RN55D ±1%, 5.36K	924-353-62	1	R42
30	RES, FILM RN55D ±1%, 7.23K	924-372-32	2	R47,R72
31	RES, FILM RN55D ±1%, 86.6K	924-386-62	1	R41
32	RES, FILM RN55D ±1%, 97.6K	924-397-62	1	R45
33	RES, FILM RN55D ±1%, 10K	924-310-02	2	R36,R37
34	RES, FILM RN55C ±1%, 2.74K	924-4274-01	2	R57,R58
35	RES, 1/8 W 1%, WW, .6	934-2010-00	1	R46
36	RES, 1/8 W .05%, WW, 224.7	934-2010-01	1	R51
37	RES, CARBON 1/4W ±5%, 56K	942-205-63	1	R33
38	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	2	R10,R18
39	RES, FLAMEPROOF 1/4W ±5%, 100	940-010-00	2	R13,R14
40	RES, CARBON 1/4W ±5%, 1.5K	942-201-52	1	R71
41	RES, CARBON 2W ±5%, 2.2K	942-5220-00	3	R3-R5
42	RES, CARBON, 1/4W ±5%, 1K	942-201-02	1	R11
43	RES, CARBON, 1/4W ±5%, 100K	942-201-04	13	R8,R9,R15,R20,R23,R5 R35,R59,R64,R73,R74,
44	RES, CARBON, 1/4W ±5%, 150	942-201-51	1	R31
45	RES, CARBON, 1/4W ±5%, 20K	942-202-03	4	R12,R16,R21,R30
46	RES, CARBON, 1/4W ±5%, 220	942-202-21	1	R65
47	RES, CARBON, 1/4W ±5%, 220K	942-202-24	2	R27,R34
48	RES, CARBON, 1/4W ±5%, 3.9K	942-203-92	1	R28

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, REED RTD FEM	MODEL NO. 235	231-4585-00	C
		DATE 7-7-83	SHEET 5 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON, 1/4W ±5%, 39K	942-203-93	1	R25
50				
51	RES, CARBON, 1/4W ±5%, 47K	942-204-73	2	R19,R26
52	RES, CARBON, 1/4W ±5%, 470K	942-204-74	3	R24,R29,R32
53				
54	RES, CARBON 1W +5%, 2.2K	942-4220-00	2	R1,R2
55	RES, CARBON 1/4W ±5%, 2.2M	942-202-25	1	R17
56	CAP, .01 µF, 50V	900-021-07	3	C3,C4,C29
57	CAP, .1 µF, 50V	900-021-08	8	C5-C7,C12,C22, C25,C27,C28
58	CAP, DISC, 100pf @ 1KV	901-011-01	1	C24
59	CAP, MONO, 22pf @ 1KV	909-002-20	1	C23
60	CAP, .001 µF, 50V	900-021-09	3	C8,C9,C18
61	CAP, PLP, .1/200V, IMB	917-001-20	1	C20
62	CAP, PLP, .22/200V, IMB	917-022-20	4	C11,C14,C17,C26
63	CAP, CER, 100pf, 50V	900-021-13	1	C13
64	CAP, CER, .0022, 50 VDC	900-021-12	1	C10
65				
66	CAP, DISC, .01/500V (5GA)	900-021-04	3	C15,C16,C30
67	RES, CARBON 1/4W ±5%, 1M	942-201-05	1	R66
68	RES, FILM RN55C ±1%, 267	924-4267-00	1	R61
69	DIODE, 1N914 (1N4148)	961-091-40	13	CR7,CR11,CR12,CR13, CR17,CR23-CR26,CR29-CR3
70	DIODE, 1N457	961-045-70	2	CR18,CR19
71	DIODE, 1N5236B	961-523-62	8	CR1-CR4,CR14, CR20,CR22,CR33
72	DIODE, 1N5233B	961-523-31	1	CR21

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, REED RTD FEM	MODEL NO. 235	231-4585-00	C
		DATE 7-7-83	SHEET 6 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	DIODE, 1N5243B	961-5243-13	2	CR27,CR28
74	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C19,C21
75	POT, 1K CERMET (72PR1K)	960-0110-43	2	R38,R48
76				
77	POT, 1M CERMET (72PR1M)	960-0110-42	1	R22
78				
79				
80	POT, 20 CERMET (66PR20)	960-0120-61	1	R62
81	POT, 1M (66PR1M)	960-0110-40	1	R49
82	POT, 10K (66PR10K)	960-0110-39	1	R50
83	FET, 2202 (NJ,L)	100-722-02	6	Q7,Q9,Q18-Q21
84	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Z5
85				
86				
87	XSTR, PN4250	962-425-00	7	Q1,Q3,Q5,Q8,Q10 Q12,Q13
88	XSTR, MPSA13	964-040-03	1	Q14
89	XSTR, MPSA18	964-0400-18	4	Q2,Q6,Q11,Q23
90				
91				
92				
93	OPTO, 4N36 (GE)(MOT)	965-5700-11	2	OC1,OC2
94				
95				
96				

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MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
ASSEMBLY, PCB, REED RTD FEM	ML	231-4585-00	C
	MODEL NO. 235	DATE 7-7-83	SHEET 7 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97				
98	XFMR, INTERFACE	967-0050-33	1	T1
99	XFMR, TOROID	967-0050-30	1	T2
100				
101				
102				
103				
104	STDF, 1/2 X 440 A2	991-020-53	4	
105	SPACER, 1/8 X 6 A2	991-020-88	3	
106	CONN, 24 PIN FEMALE	973-3600-24	1	J1
107	CONN, 24 PIN MALE	973-0101-52	1	P1
108				
109	REED RELAY, 3 FORM A	000-8044-00	20	K2-EVEN NO. THRU K40
110	REED RELAY, 2 FORM A	000-8210-00	20	K1-ODD NO. THRU K39
111				
112				
113				
114				
115				
116				
117				
118				
119	TERMINAL STRIP, 10 PIN	973-0101-51	8	TB1-TB4
120				

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X3	R & D RELEASE	—	--	--
		A1	LTD. SAGE REL PER EO 2-1140-4	[illegible]	[illegible]	[illegible]
		B	PROD. REL PER E.O.# 11520	[illegible]	[illegible]	[illegible]

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.
2. RESISTANCE IN OHMS, 1/4 WATT, ±5%.
3. CAPACITANCE IN MF.

(4) R1 THRU R40 ARE 2.2K, 1/2 WATT.

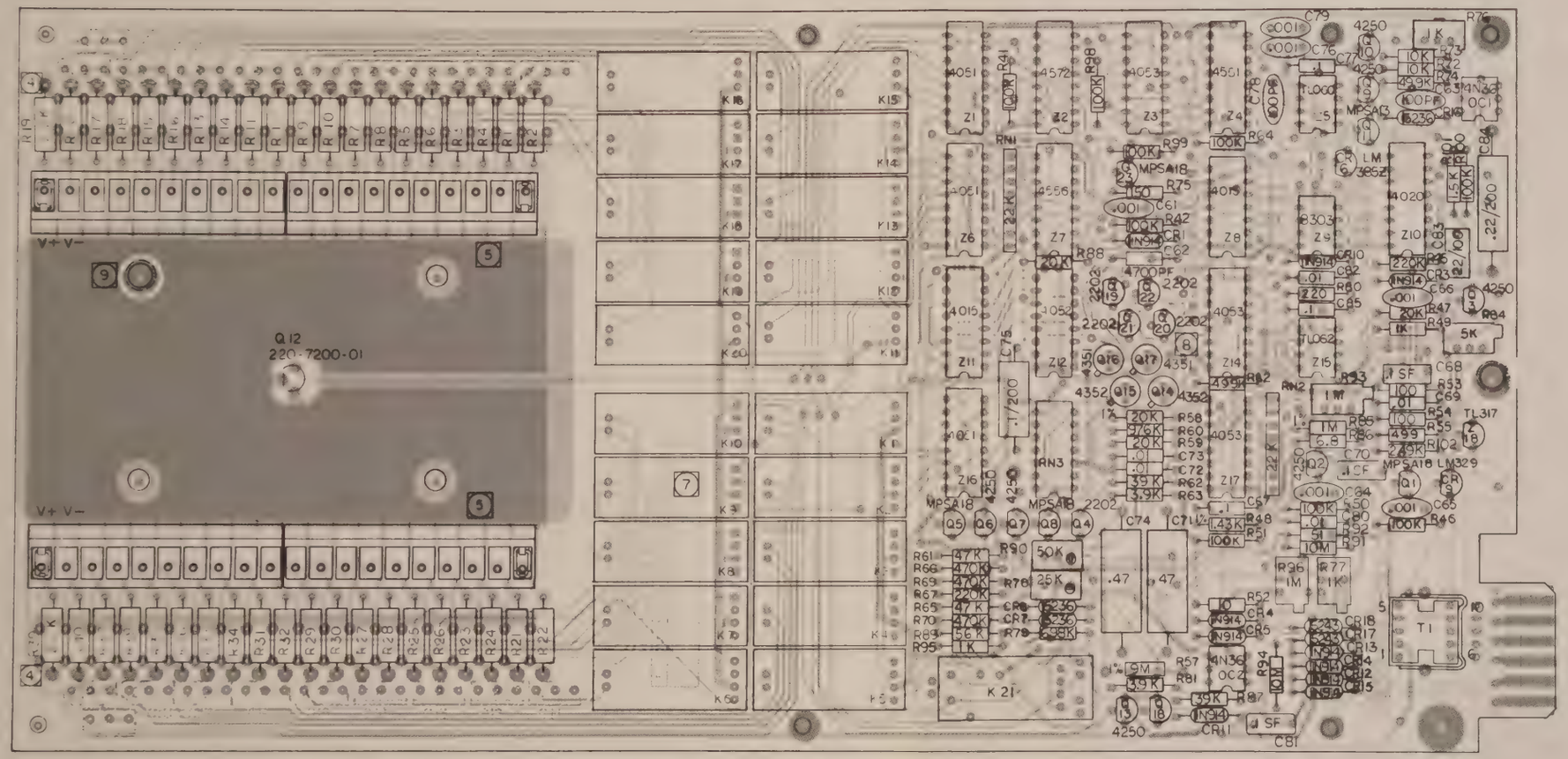
(5) INSTALL TERMINAL STRIP (ITEM 89), 4 PLACES.

(6) INSTALL 1/8" LONG SPACER (ITEM 90) ON SOLDER SIDE.

(7) RUBBER STAMP ASSEMBLY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON SLDR SIDE.

(8) DO NOT REMOVE SHORTING CLIPS FROM Q14, Q15, Q16 AND Q17 UNTIL ITEMS ARE SOLDERED TO BOARD.

(9) INSTALL STAND-OFF # 6-32 X .125 LG (ITEM 63) ON SOLDER SIDE. (SOLDER TO CLAD)



ASSEMBLY NO	SUPERSEDES			DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO, CA 92123			
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	DRAWN	S. DUONG	6-84				
	CHECK	[illegible]	6/12/84				
	APPR.	[illegible]	[illegible]		SCALE	DO NOT SCALE DRAWING	SHEET 1 OF 6

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES IN OHMS, 1/4WATT, ±5%.
2. CAPACITANCE VALUES IN MICROFARAD.
3. RESISTORS R1 THRU R40 ARE 2.2K, 1/2W, ±5%.
4. CAPACITORS C1 THRU C20 ARE .22MF, SF @ 100V.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X1	R & D RELEASE			
		X2	R & D RELEASE		-	
		A1	I.T.D. USAGE REL. PER E.O. 2-11464			
		B	PROD. REL. PER E.O. 2-11520			

REF DESIGNATION		
LAST USED		DO NOT USE
RESISTOR	R102	R43,R44,R56,R68,R71,R83
CAPACITOR	C85	C1-C60
DIODE	CR18	CR2
TRANSISTOR	Q23	
TRANSFORMER	T1	
RES NETWORK	RN3	
RELAY	K21	
IC	Z18	
OPTO-COUPLER	OC2	

ASSEMBLY NO. 231-4180-XX	SUPERSEDES	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO CA 92123
DES/ENG		TITLE: SCHEMATIC, PRGM ATTEN REED FEM
DRAWN S. DUONG 11-2-83		SIZE D
CHECK 12/7/83		DRAWING NO. 231-6180-00
APPR.		CHANGE LETTER B
		SCALE DO NOT SCALE DRAWING SHEET 1 OF 2

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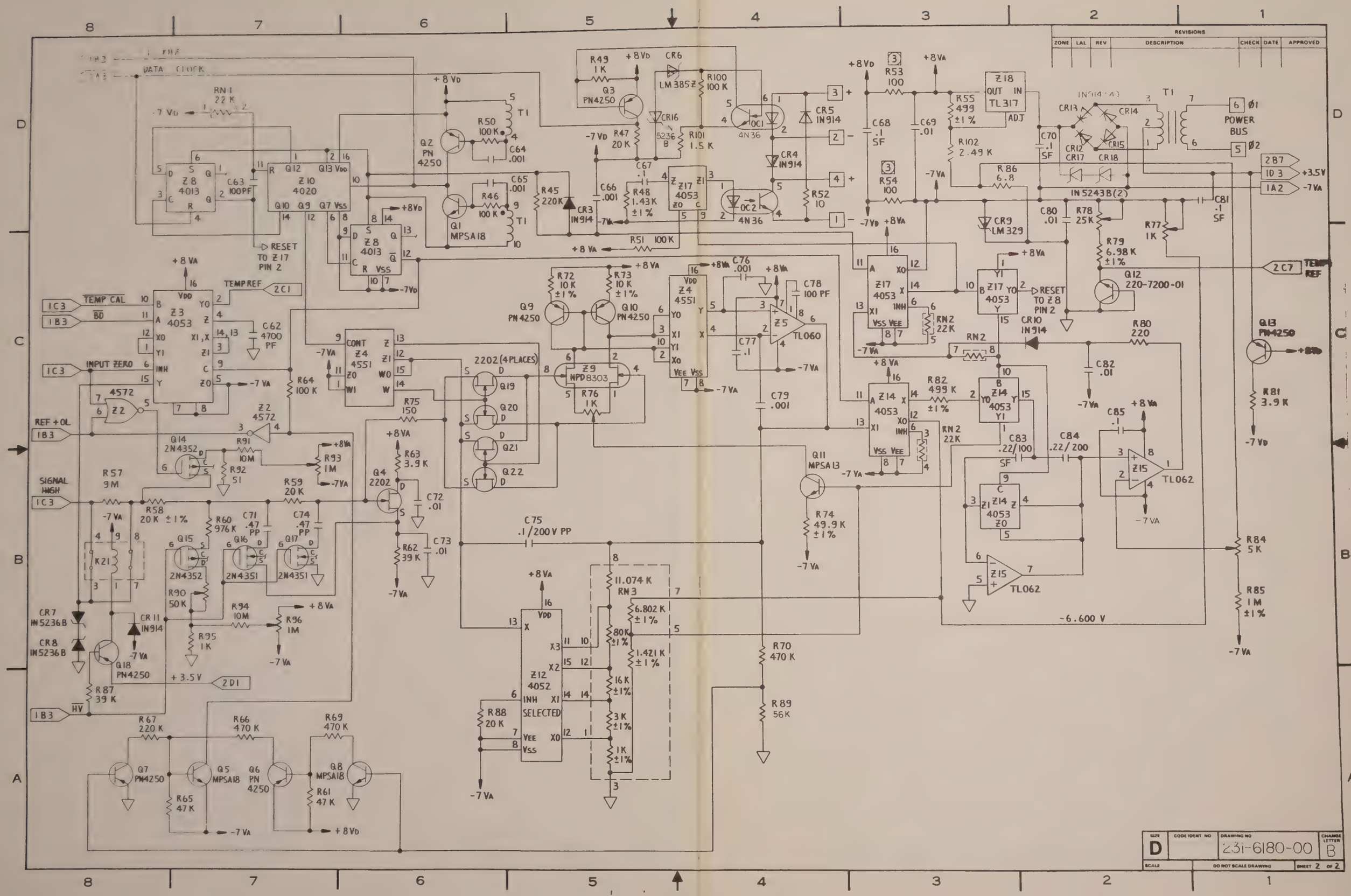

REVISIONS
ZONE LAL REV DESCRIPTION CHECK DATE APPROVED
DATA CLOCK
RN1 22K
Z8 4013
Z10 4020
Z8 4013
RESET TO Z17 PIN 2
Q2 PN 4250
Q1 MPSA18
R50 100K
R46 100K
C64 .001
C65 .001
R45 220K
CR3 IN914
R49 1K
Q3 PN4250
CR6 LM385Z
R100 100K
CR16 5236B
R47 20K
R101 1.5K
C66 .001
C67 .1
R48 1.43K ±1%
Z17 4053
R51 100K
OC1 4N36
OC2 4N36
CR5 IN914
CR4 IN914
R52 10
R53 100
R54 100
C68 .1 SF
C69 .01
R55 499 ±1%
R102 2.49K
Z18 TL317
ADJ
C70 .1 SF
CR13 CR14 CR12 CR15 CR17 CR18
IN914(4)
T1
POWER BUS
Ø1
Ø2
2B7
1D3
1A2
+3.5V
-7VA
R86 6.8
IN5243B(2)
C81 .1 SF
C80 .01
R78 25K
R79 6.98K ±1%
R77 1K
CR9 LM329
Q12 220-7200-01
2C7 TEMP REF
Z17 4053
RESET TO Z8 PIN 2
CR10 IN914
RN2 22K
R80 220
C82 .01
Q13 PN4250
R81 3.9K
R84 5K
R85 1M ±1%
Z3 4053
TEMP CAL
BD
INPUT ZERO
TEMP REF
2C1
C62 4700 PF
R64 100K
Z4 4551
CONT
Z2 4572
REF + OL
Q14 2N4352
R91 10M
R92 51
R93 1M
SIGNAL HIGH
R57 9M
R58 20K ±1%
R59 20K
R60 976K
C71 .47 PP
C74 .47 PP
Q15 2N4352
Q16 2N4351
Q17 2N4351
K21
R90 50K
R94 10M
R96 1M
R95 1K
CR7 IN5236B
CR8 IN5236B
CR11 IN914
Q18 PN4250
+3.5V
2D1
R87 39K
HV
R67 220K
R66 470K
R69 470K
Q7 PN4250
Q5 MPSA18
Q6 PN 4250
Q8 MPSA18
R65 47K
R61 47K
R72 10K ±1%
R73 10K ±1%
Q9 PN4250
Q10 PN4250
Z9 NPD8303
R76 1K
2202 (4 PLACES)
Q19
Q20
Q21
Q22
R75 150
Q4 2202
R63 3.9K
C72 .01
R62 39K
C73 .01
C75 .1/200V PP
Z4 4551
C76 .001
C78 100 PF
Z5 TL060
C77 .1
C79 .001
Z12 4052
SELECTED
R88 20K
11.074K RN3
6.802K ±1%
80K ±1%
1.421K ±1%
16K ±1%
3K ±1%
1K ±1%
R70 470K
R89 56K
Q11 MPSA13
R74 49.9K ±1%
Z14 4053
R82 499K ±1%
RN2 22K
C83 .22/100 SF
C84 .22/200
C85 .1
Z15 TL062
-6.600 V
SIZE D
CODE IDENT NO
DRAWING NO 231-6180-00
CHANGE LETTER B
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 2

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV
PCB ASSEMBLY, REED (PROGRAMMABLE) ATTENUATOR FEM	ML	231-4180-00	B
	MODEL NO. 235	DATE 11-7-83	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, REED ATTENUATOR FEM	231-2180-00	1	
2	SCHEMATIC, REED ATTENUATOR FEM	231-6180-00	1	
3	TEST SPEC			
4				
5				
6	IC, 4051 8 CHAN MUX (NL)	965-587-77	3	Z1,Z6,Z16
7	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z11
8	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z8
9	IC, 4556 DUAL 1OF4 DEC(MO,FC,NL)	965-587-48	1	Z7
10	IC, 4053 TRIPLE 2-CHAN MUX (M)	965-5870-81	3	Z3,Z14,Z17
11	IC, 4020 14 BIT BIN CTR (RCA)	965-5870-84	1	Z10
12	IC, TL060 OPAMP (TI)	965-646-00	1	Z5
13	IC, TL062 DUAL OPAMP (TI)	965-6170-03	1	Z15
14	IC, TL317 REG	965-645-00	1	Z18
15	IC, 4052 DUAL 4-CHAN MUX, SELEC.	000-8051-00	1	Z12
16				
17	IC, 4551 4-2 CHAN MUX	965-5870-82	1	Z4
18	IC, 4572 INV, NOR, NAND, CMOS	965-618-00	1	Z2
19				
20	RES, CARBON 1/4W ±5%, 10M	942-201-06	2	R91,R94
21	RES, CARBON 1/4W ±5%, 10	942-201-00	1	R52
22	RES, RN55D ±1%, 20K	924-320-02	1	R58
23	RES, RN65C ±.1%, 9M	922-590-04	1	R57
24	RES, RN55E ±.1%, 976K	922-4976-02	1	R60

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED (PROGRAMMABLE) ATTENUATOR FEM	MODEL NO. 235	DATE 11-7-83	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D ±1%, 1.43K	924-314-30	1	R48
26	RES, FILM RN55C ±1%, 499K	924-4499-20	1	R82
27	RES, FILM RN55D ±1%, 499	924-349-90	1	R55
28	RES, FILM RN55C ±1%, 6.98K	924-469-81	1	R79
29	RES, FILM RN55D ±1%, 10K	924-310-02	2	R72,R73
30	RES, FILM RN55C ±1%, 49.9K	924-3499-10	1	R74
31	RES, FLAMEPROOF 1/4W 5%, 100	940-010-00	2	R53,R54
32	RES, FILM RN55C ±1%, 2.49K	924-4249-01	1	R102
33	RES, CARBON 1/4W ±5%, 1K	942-201-02	2	R49,R95
34	RES, CARBON 1/4W ±5%, 100K	942-201-04	9	R41,R42,R46,R50, R51,R64,R98-R100
35	RES, CARBON 1/4W ±5%, 150	942-201-51	1	R75
36	RES, CARBON 1/4W ±5%, 20K	942-202-03	3	R47,R59,R88
37	RES, CARBON 1/4W ±5%, 220	942-202-21	1	R80
38	RES, CARBON 1/4W ±5%, 220K	942-202-24	2	R45,R67
39	RES, CARBON 1/4W ±5%, 3.9K	942-203-92	2	R63,R81
40	RES, CARBON 1/4W ±5%, 39K	942-203-93	2	R62,R87
41	RES, CARBON 1/4W ±5%, 6.8	942-206-89	1	R86
42	RES, CARBON 1/4W ±5%, 1.5K	942-201-52	1	R101
43	RES, CARBON 1/4W ±5%, 47K	942-204-73	2	R61,R65
44	RES, CARBON 1/4W ±5%, 470K	942-204-74	3	R66,R69,R70
45	RES, CARBON 1/2W ±5%, 2.2K	942-302-22	40	R1-R40
46	RES, CARBON 1/4W ±5%, 56K	942-205-63	1	R89
47	RES, CARBON 1/4W ±5%, 51	942-205-10	1	R92
48	RES, CARBON 1/4W ±5%, 1M	942-201-05	1	R85

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED (PROGRAMMABLE) ATTENUATOR FEM	MODEL NO. 235	DATE 11-7-83	231-4180-00 B
		SHEET 5 OF 6	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	CAP, .01 50V (180175H050A)	900-021-07	5	C69,C72,C73,C80, C82
50	CAP, .1 50V AXIAL	900-021-08	3	C67,C77,C85
51	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	6	C61,C64-C66,C76, C79
52	CAP, DISC, 100pf @ 1KV (5GA)	901-011-01	2	C63,C78
53				
54	CAP, PLP, .1/200V, IMB(GA2C104K)	917-001-20	1	C75
55	CAP, PLP,.22/200V, IMB(GA2C224K)	917-022-20	1	C84
56	CAP, PLP,.47/200V, IBM(GA2C474K)	917-047-20	2	C71,C74
57				
58	CAP, SF, .1/100V, SMS (B32570)	918-001-10	3	C68,C70,C81
59	CAP, MONO, 4700pf	909-470-00	1	C62
60	CAP, SF, .22/100V, SMS (B32570)	918-022-10	1	C83
61				
62				
63	STAND-OFF .250 DIA 6-32 X.125LG	991-020-67	1	
64				
65				
66				
67	DIODE, 1N5243B	961-5243-13	2	CR17,CR18
68	DIODE, 1N5236B	961-523-62	3	CR7,CR8,CR16
69	DIODE, 1N914 (1N4148)	961-091-40	10	CR1,CR3-CR5, CR10-CR15
70	DIODE, LM385Z	961-385-00	1	CR6
71	DIODE, LM329	965-636-00	1	CR9
72				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED (PROGRAMMABLE) ATTENUATOR FEM	MODEL NO. 235	DATE 11-7-83	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	MOS FET, 2N4351 N CHAN	963-4351-00	2	Q16,Q17
74	MOS FET, 2N4352 P CHAN	963-4352-00	2	Q14,Q15
75	RELAY REED 2 FORM (B) (2K)	000-8211-00	1	K21
76	TRANSISTOR (SELECTED-COLOR DOT)	220-7200-01	1	Q12
77	RELAY, REED LOW THERMAL (2K)	000-8210-00	20	K1-K20
78	FET, 2202 (NJ,LO-LK,GP)	100-722-02	5	Q4,Q19-Q22
79	TRANSFORMER, INTERFACE	967-0050-33	1	T1
80	RES, NTWK 22K (708B223)	950-0220-00	2	RN1,RN2
81	RES, NTWK FEM	230-7100-00	1	RN3
82	POT, 1K (68X)	960-0110-45	1	R77
83	POT, 1K CERMET (72XL)	960-011-25	1	R76
84	POT, 25K MT2X253	960-015-15	1	R78
85	XSTR, PN4250 (PNPA)(FC,NL)	962-425-00	8	Q2,Q3,Q6,Q7,Q9, Q10,Q13,Q18
86	XSTR, MPSA13	964-040-03	1	Q11
87	XSTR, MPSA18	964-0400-18	4	Q1,Q5,Q8,Q23
88	XSTR, FET NPD 8303 DUAL N CHAN	962-8303-00	1	Z9
89	TERMINAL STRIP 10PIN	973-0101-51	4	
90	SPACER, .250 DIA X .125 LG	991-020-88	1	
91	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	6	
92	OPTO, 4N36 (GE)(MOT)	965-5700-11	2	OC1,OC2
93	POT, 50K	960-015-17	1	R90
94	POT, 5K	960-0150-22	1	R84
95				
96	POT, 1M (68X)	960-0110-44	2	R93,R96

13 RUBBER STAMP ASSEMBLY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR (SLDR) SIDE.

14. ALL TRANSISTORS 1/4" HIGH MAX.

15 C82 1/4" HIGH MAX.

7 INSTALL 1/8" LONG STANDOFF (ITEM 93) ON SOLDERSIDE.

8 INSTALL 7/16" LONG STANDOFF (ITEM 92) ON COMPONENT SIDE.

9 INSTALL CONNECTOR (ITEM 101) ON COMPONENT SIDE.

10 BREAK ALONG SLOT AND TRIM EDGE OF BOARDS FLUSH, (EDGE OF BOARDS STRAIGHT).

11 INSTALL CONNECTOR (ITEM 102) ON COMPONENT SIDE.

12 TO CONNECT THE BOARD HALVES TOGETHER, WITH COMPONENTS FACING EACH OTHER, INSERT CONN (ITEM 102) INTO CONN SOCKET (ITEM 101). INSTALL SHIELD (ITEM 106) TO THE TOP BOARD WITH CLAD SIDE UP USING SCREW 4-40 X 5/16 (ITEM 98), WASHER SPLITLOCK (ITEM 96), WASHER FLAT (ITEM 97) 4 EACH.

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.

2 R1-R40, R104-R163 ARE 2.2K, 1/2WATT.

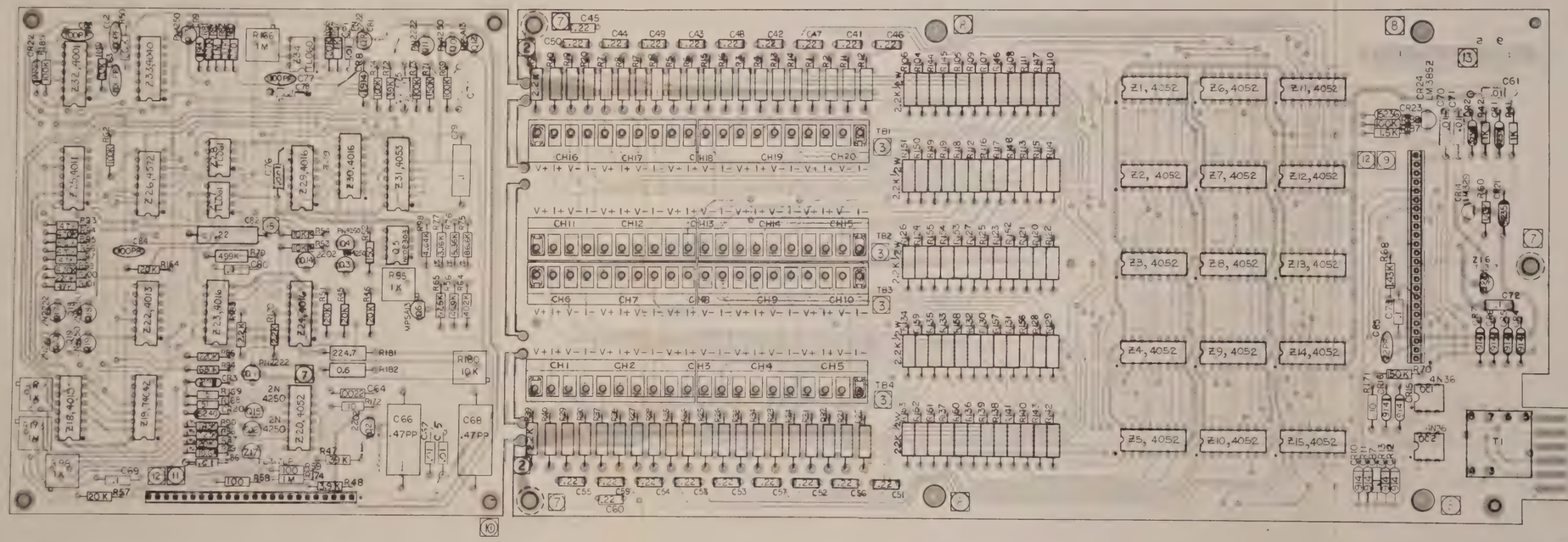
3 INSTALL TERMINAL STRIP (ITEM 104), 8 PLACES.

4 DELETED.

5. RESISTANCE IN OHMS, 1/4 WATT, ± 5%.

6. CAPACITANCE IN MF.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A1	LIMITED USAGE RELEASE PER E.O. 2-11366			
		A2	REVISED PER E.O. 2-11448			
		B	PROD. REL. PER E.O. 2-11483			
		B	REVISED PER E.O. 2-11614			



HOLE TOLERANCES	NOTES UNLESS SPECIFIED	DRAWN	6-16-83
000 .250 DIA. + .004 .002 251 .500 DIA. + .005 .002 501 1.00 DIA. + .010 .005	1. TOLERANCES XX ± .03 DIMENSIONED ANGLES XXX ± .010 ± ½° 2. BREAK ALL SHARP EDGES .010 APPROX 3. MACH. SURFACES 4. ALL DIM. IN INCHES 5. ALL TRUE POSITION TOLERANCES APPLY AT MMC	CHECK	2-16-83
SUPERSEDES		APPR	1/4/83
		MATERIAL	
	USED ON: 235	FINISH	
	NEXT ASSY 231-5601 -XX		

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3800 RUFFIN ROAD • SAN DIEGO, CA 92123

TITLE: ASSEMBLY PCB LOW POWER RTD FEM

SIZE	CODE IDENT NO	DRAWING NO	CHANGE LETTER
D		231-4601-01	B

SCALE 1:1 | DO NOT SCALE DRAWING | SHEET 1 OF 7

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES IN OHMS, 1/4W, ±5%
2. CAPACATANCE VALUES IN MICROFARAD.
3. ALL DIODES ARE 1N914.
4. RESISTORS R1 THROUGH R40 AND R104 THROUGH R163 ARE 2.2K, 1/2W, ±5%.
5. DELETED.
6. CAPACITORS C41 THROUGH C60 ARE .22 MF SF @ 100V.
7. INDICATES CONNECTIONS BETWEEN BOARD 1 AND BOARD 2. 7, 11, 15 AND 16 ARE SPARES.
8. THIS RESISTOR MUST BE FLAMEPROOF.

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A	LTD USAGE REL PER E.O. 2-11366			
		B	REVISED PER E.O. 2-11448			
		C	PROD. REL. PER E.O. 2-11483			

REFERANCE DESIGNATOR CHART

REF. DESIG.	LAST USED	UNUSED
RESISTORS	R188	R43,44,61,63,78,91,92,102, 103,165,175,176,177,178,179
CAPACITORS	C88	C83
TRANISTORS	Q20	Q7, Q9
I.C.'S	Z34	Z21
DIODES	CR24	CR17, 18, 19
OPTO-COUPLER	OC2	
TRANSFORMER	T1	
TERM-BLOCKS	TB4	

ASSEMBLY NO. 231-4601-XX

SUPERSEDES

DES/ENG	R. Ruiz	3/15/84
DRAWN	K. Foster	6/7/83
CHECK	[illegible]	3/19/84
APPR.	[illegible]	4/4/84

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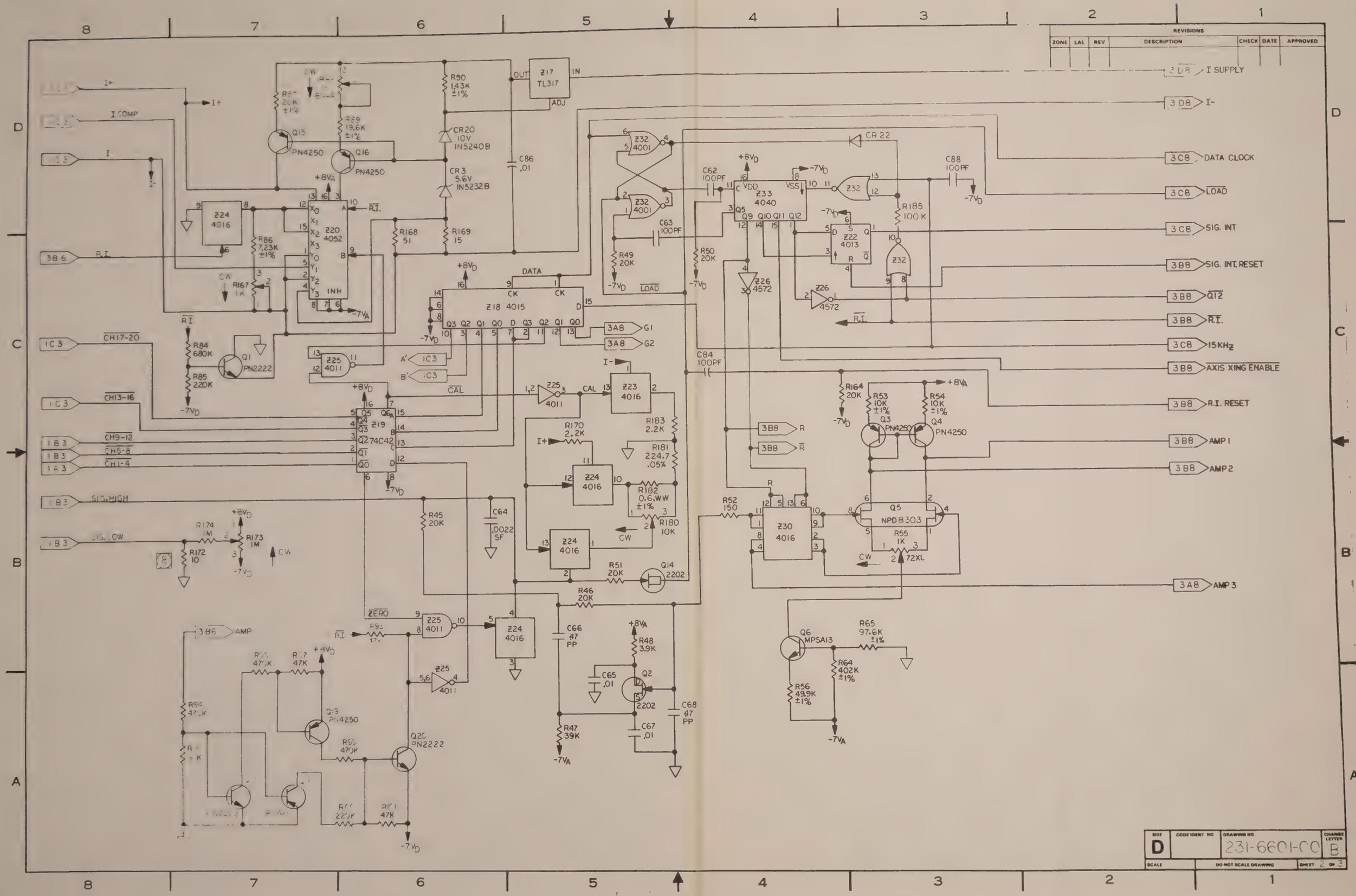
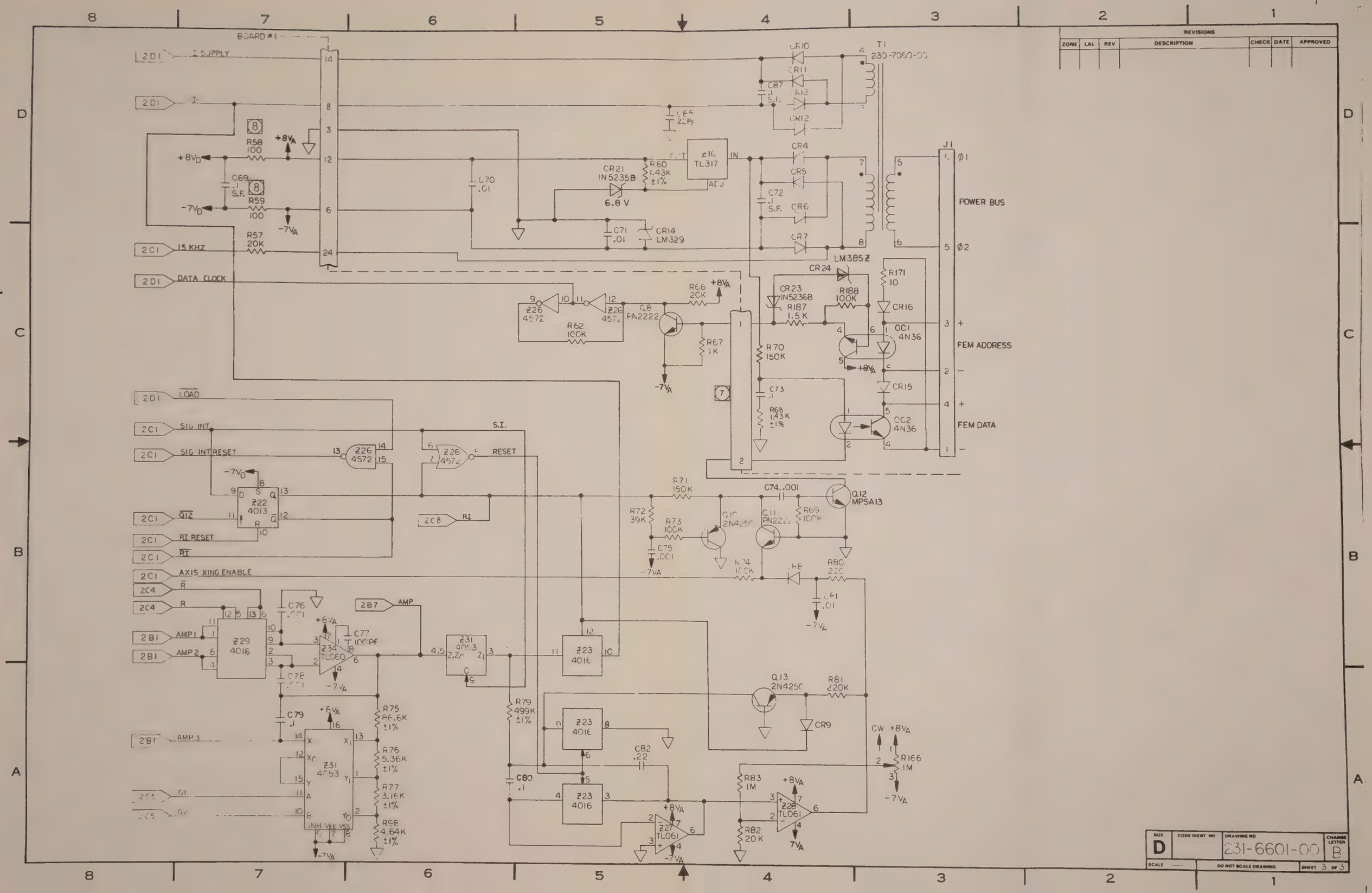
TITLE: SCHEMATIC LOW POWER INTERFACE

SIZE: D | DRAWING NO. 231-6601-00 | CHANGE LETTER: B

SCALE: - | DO NOT SCALE DRAWING | SHEET 1 OF 3



REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
I SUPPLY
I-
DATA CLOCK
LOAD
SIG. INT
SIG. INT. RESET
Q12
R.I.
15KHz
AXIS XING ENABLE
R.I. RESET
AMP 1
AMP 2
AMP 3
I COMP
R.I.
CH17-20
CH13-16
CH9-12
CH5-8
CH1-4
SIG. HIGH
SIG. LOW
AMP
Z17 TL317
Z20 4052
Z18 4015
Z19 74C42
Z23 4016
Z24 4016
Z25 4011
Z26 4572
Z30 4016
Z32 4001
Z33 4040
Z22 4013
Q1 PN2222
Q2 2202
Q3 PN4250
Q4 PN4250
Q5 NPD8303
Q6 MPSA13
Q14 2202
Q19 PN4250
Q20 PN2222
CR20 10V IN5240B
CR3 5.6V IN5232B
CR 22
R90 1.43K ±1%
R89 19.6K ±1%
R86 7.23K ±1%
R167 1K
R168 51
R169 15
R84 680K
R85 220K
R45 20K
R46 20K
R47 39K
R48 3.9K
R49 20K
R50 20K
R51 20K
R52 150
R53 10K ±1%
R54 10K ±1%
R55 1K 72XL
R56 49.9K ±1%
R64 402K ±1%
R65 97.6K ±1%
R164 20K
R170 2.2K
R181 224.7 .05%
R182 0.6,WW ±1%
R183 2.2K
R180 10K
R185 100K
R174 1M
R173 1M
R172 10
R95 470K
R97 47K
R99 470K
R101 47K
R96 470K
R100 220K
C86 .01
C64 .0022 SF
C62 100PF
C63 100PF
C88 100PF
C84 100PF
C66 47 PP
C65 .01
C67 .01
C68 47 PP
CAL
ZERO
DATA
CW
SIZE
D
CODE IDENT NO
DRAWING NO.
231-6601-00
CHANGE LETTER
B
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 3



REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

SIZE	CODE IDENT NO	DRAWING NO	CHANGE LETTER
D		231-6601-00	B
SCALE —		DO NOT SCALE DRAWING	SHEET 3 OF 3

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, LOW POWER RTD FEM		231-4601-01	B
	MODEL NO. 235	DATE 6-14-83	SHEET 3 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, LOW POWER RTD FEM	231-2601-01	1	
2	SCHEMATIC, LOW POWER RTD FEM	231-6601-00	1	
3	TEST SPEC			
4				
5				
6	IC, TL 317LP VREG (TI)	965-645-00	2	Z16,Z17
7				
8	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z32
9	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z25
10	IC, 4015 DUAL SE CMOS (MO)	965-587-03	1	Z18
11				
12	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z22
13	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z19
14	IC, 4040 12 BIT BIN CTR (MO,FC)	965-587-46	1	Z33
15	IC, 4572 INV, NOR, NAND CMOS(MO)	965-618-00	1	Z26
16	IC, TL060CP OPAMP (TI)	965-646-00	1	Z34
17	IC, TL061CP OPAMP (TI)	965-646-01	2	Z27,Z28
18	IC, 4053 3-2 CHAN MUX	965-5870-81	1	Z31
19				
20				
21	RES, FILM RN55D 1%, 49.9K	924-3499-10	1	R56
22	RES, FILM RN55D 1%, 97.6K	924-397-62	1	R65
23	RES, FILM RN60C 1%, 499K	920-449-93	1	R79
24	RES, FILM RN55D 1%, 10K	924-310-02	2	R53,R54

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, LOW POWER RTD FEM	MODEL NO. 235	231-4601-01	B
	DATE 6-14-83	SHEET 4 OF 7	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D 1%, 1.43K	924-314-30	3	R60,R68,R90
26	RES, FILM RN55D 1%, 19.6K	924-319-62	1	R89
27	RES, FILM RN55D 1%, 20K	924-320-02	1	R87
28	RES, FILM RN55D 1%, 3.16K	924-331-61	1	R77
29	RES, CARBON 1/4W, ±5%, 1.5K	942-201-52	1	R187
30	RES, FILM RN55D 1%, 4.64K	924-346-41	1	R98
31	RES, FILM RN55D 1%, 5.36K	924-353-62	1	R76
32	RES, FILM RN55D 1%, 402K	924-340-23	1	R64
33	RES, FILM RN55D 1%, 7.23K	924-372-32	1	R86
34	RES, FILM RN55D 1%, 86.6K	924-386-62	1	R75
35	RES, 1/8W, 1%, WW 0.6	934-2010-00	1	R182
36	RES, 1/8W, .05% WW 224.7	934-2010-01	1	R181
37	RES, FLAMEPROOF 1/4W, 100	940-010-00	2	R58,R59
38	RES, CARBON 1/4W ± 5%, 1K	942-201-02	3	R41,R42,R67
39	RES, CARBON 1/4W ± 5%, 100K	942-201-04	6	R62,R69,R73,R74, R185,R188
40	RES, CARBON 1/4W ± 5%, 15	942-201-50	1	R169
41	RES, CARBON 1/4W ± 5%, 150	942-201-51	1	R52
42	RES, CARBON 1/4W ± 5%, 150K	942-201-54	2	R70,R71
43	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45,R46,R49-51, R57,R66,R82,R164
44	RES, CARBON 1/4W ± 5%, 220	942-202-21	1	R80
45	RES, CARBON 1/4W ± 5%, 220K	942-202-24	3	R81, R85,R100
46	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
47	RES, CARBON 1/4W ± 5%, 39K	942-203-93	2	R47,R72
48	RES, FLAMEPROOF 1/4W ± 5%, 10	940-001-00	1	R172

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, FRONT PANEL BOARD	MODEL NO. 235	DATE 4-[illegible]-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, FRONT PANEL BOARD	231-2320-00	1	
2	SCHEMATIC	231-6320-00	1	
3	TEST SPEC			
4				
5				
6	IC, 4001 4-2IN NOR CMOS	965-587-01	1	4B
7	IC, 4017 COUNTER/DIV CMOS (MO)	965-587-18	2	2C,4C
8	IC, 74C221 DUAL MONO(FC,NL,MO)	965-587-45	2	1E,4A
9	IC, 4040 12BIT BIN CTR	965-587-46	2	3C,3D
10	IC, 4503 TRI-STATE HEX BUFFER	965-587-69	1	4D
11	IC, 74C907 OPEN D PMOS HEX BUF	965-587-71	2	2B,2D
12	IC, 4010 CMOS BUFFER	965-587-73E	1	2A
13	IC, ULN2003A,7DARL ARRAY(SPFMO)	965-625-01	6	1B,1C,1D,2E,3E, 4E
14	IC, 74LS175 QUAD D F/F	965-635-46	1	3B
15				
16				
17				
18				
19				
20	RES, CARBON 1/4W ± 5%, 10	942-201-00	8	R16-R23
21	RES, CARBON 1/4W ± 5%, 1K	942-201-02	1	R45
22	RES, CARBON 1/4W ± 5%, 10K	942-201-03	14	R31-R35,R37,R39 R43,R27-30,R46,R6
23	RES, CARBON 1/4W ± 5%, 20K	942-202-03	5	R11-R15
24	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	3	R7, R41,R42

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, FRONT PANEL BOARD	MODEL NO. 235	231-4320-00	E
	DATE 4-15-82	SHEET 4 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26				
27	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	5	R8,R9,R10,R47 R38
28	RES, CARBON 1/4W ± 5%, 47K	942-204-73	3	R25,R26,R1
29				
30	RES, CARBON 1/4W ± 5%, 820	942-208-21	1	R3
31	RES NWK, 2.2K 16 DIP (898-3-R2.2K)	951-022-01	1	RN1
32				
33	RES, CARBON 1/4W ± 5%, 330	942-203-31	2	R24,R40
34	RES, CARBON 1/4W ± 5%, 100K	942-201-04	1	R36
35				
36				
37	CAP, .1MF@50V(3429-050E-104Z)A	900-021-02	1	C1
38	CAP, .01/50V 1801Z5U050A	900-021-07	24	C7,C9,C11,C13-C31,C32,C3
39	CAP, 1UF @ 50V (196D)	916-010-05	2	C5,C2
40	CAP, 10MF @ 10V (162D)	916-010-10	4	C4,C8,C10,C12
41	CAP, 22UF @ 35V (196D)	916-220-05	1	C6
42				
43				
44				
45				
46				
47	DIODE, 1N702 (3.2V) (TD,MO)	961-070-20	1	CR2
48	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	26	CR1,CR3-CR27

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

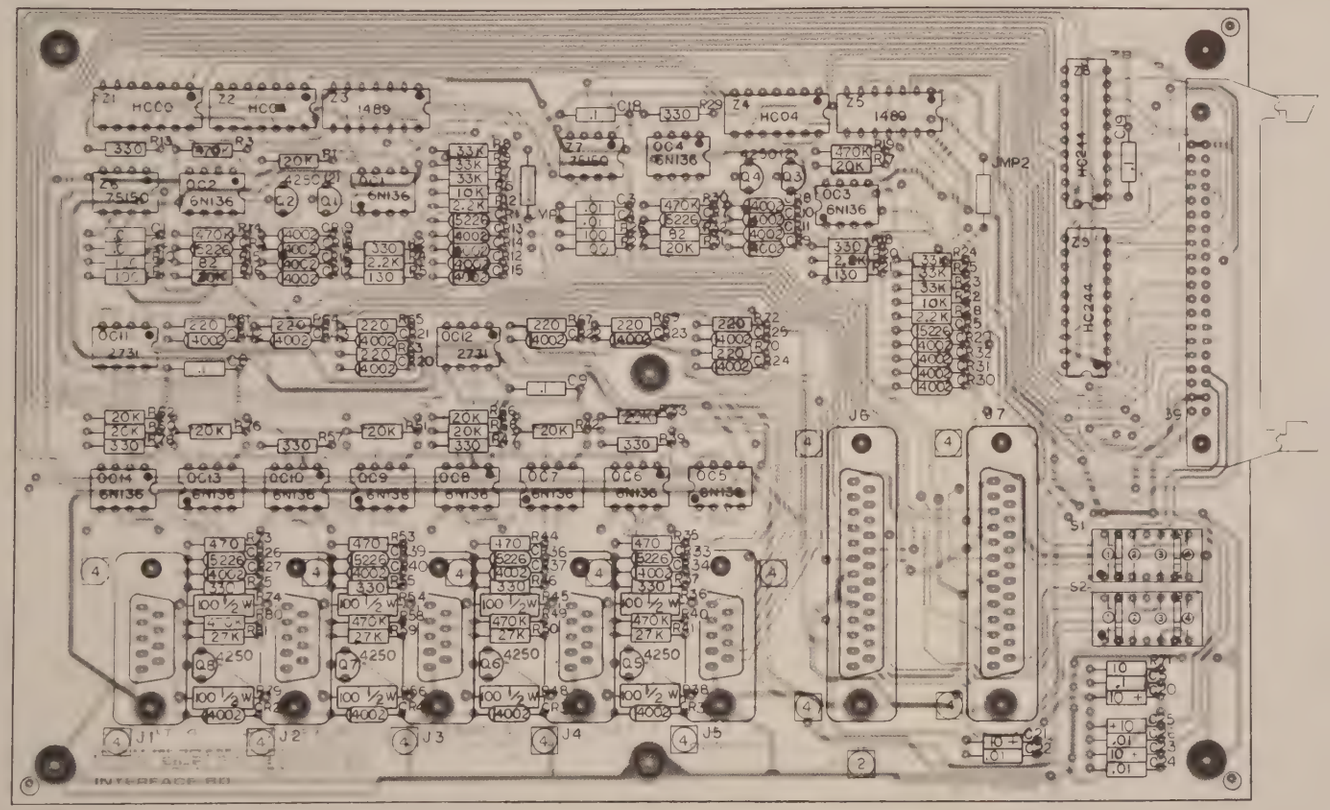
DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, FRONT PANEL BOARD	MODEL NO. 235	DATE 4-15-82	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52				
53				
54	THERMISTER 100 K JT51J5(FENWAL)	955-001-04	1	R5
55	POT, 10K CERMET 72PL	960-101-03	1	R44
56				
57	POT, 5K CERMET 72PL	960-100-53	1	R4
58	XSTR, PN2222 (NPNA92) (NA)	962-222-20	2	Q21,Q22
59	XSTR, PN2907 (PNP) (NSC)	962-290-70	18	Q3-Q20
60	XSTR, 2N4250 (PNPA) (FC,NL)	962-425-00	2	Q1,Q2
61	XSTR, MJE700, (PNPA77)(NA,MO)	964-047-00	5	Q23-Q27
62	LED, RED (MV5753)	968-010-11	8	DS10-DS17
63	DISPLAY, 1 DIGIT LED, MAN 6680	968-084-01	9	DS1-DS9
64	SWITCH DIP-4P SEALED(GH76SB04S)	969-050-12	3	S1,S2,S3
65	CONN, 17PC/FC HBLB17S3 BURNDY	973-010-48	1	J4
66	CONN PC 50 RIBBON (3M3433-2203)	973-060-10	1	P1
67	TERM STICK 8M (65610-108) BERG	973-381-00	1	P3
68	CONN, 12 PIN MOLEX 15-25-4121	973-370-11	1	J2
69	XDUCER, CERAMIC SK-173	994-001-00	1	Y1
70	SOLID 24 AWG, TEFLON INS WIRE	978-300-00	2"	Y1
71				
72				

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.
2. RUBBER STAMP ASSEMBLY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR (SOLDER) SIDE.
3. FOR MATERIAL LIST, SEE SHEETS 2 THRU 4.
4. INSTALL SWAGE STANDOFF (ITEM 48) COMP SIDE BEFORE INSTALLING CONNECTORS J1-J7.
5. MAXIMUM HEIGHT OF TRANSISTORS Q1-Q8 TO BE .300.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X2	R & D RELEASE			
		X3	R & D RELEASE			
		A1	LTD USAGE REL PER E.O. 2-11431			
		A2	REVISED PER E.O. 2-11441			
		B	PROD. REL. PER E.O. 2-11453			



HOLE TOLERANCES	NOTES UNLESS SPECIFIED			
000-250 DIA +.004 -.002 251-500 DIA +.006 -.002 501-1.00 DIA +.010 -.006	1 TOLERANCES XX ± .03 DIMENSIONED ANGLES XXX ± .010 ± ½° 2 BREAK ALL SHARP EDGES .010 APPROX 3 MACH SURFACES 4 ALL DIM IN INCHES 5 ALL TRUE POSITION TOLERANCES APPLY AT MMC	DRAWN		2-83
SUPERSEDES		CHECK		3-84
		APPR		5-84
		MATERIAL		
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DORIC DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO

TITLE: ASSEMBLY, PCB, INTERFACE BD

SIZE	CODE IDENT. NO.	DRAWING NO.	CHANGE LETTER
D		245-4100-00	B

SCALE | DO NOT SCALE DRAWING | SHEET OF 4

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. CAPACITOR VALUES ARE IN MICROFARADS.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X3	R & D RELEASE			
		A1	LTD USAGE REL PER E.O. 2-11431			
		B	PROD. REL. PER E.O. 2-11453			

REF DESIGNATION	
LAST USED	DO NOT USE
RESISTOR R81	R34,R43,R52,R77
CAPACITOR C26	C7
DIODE CR43	CR2,CR4,CR6
TRANSISTOR Q8	
OPTO-COUPLER OC14	
IC Z9	
CONNECTOR P1	
CONNECTOR J7	
SWITCH S2	
JUMPER JMP2	

ASSEMBLY NO. 245-4100-00	SUPERSEDES	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO CA 92123	
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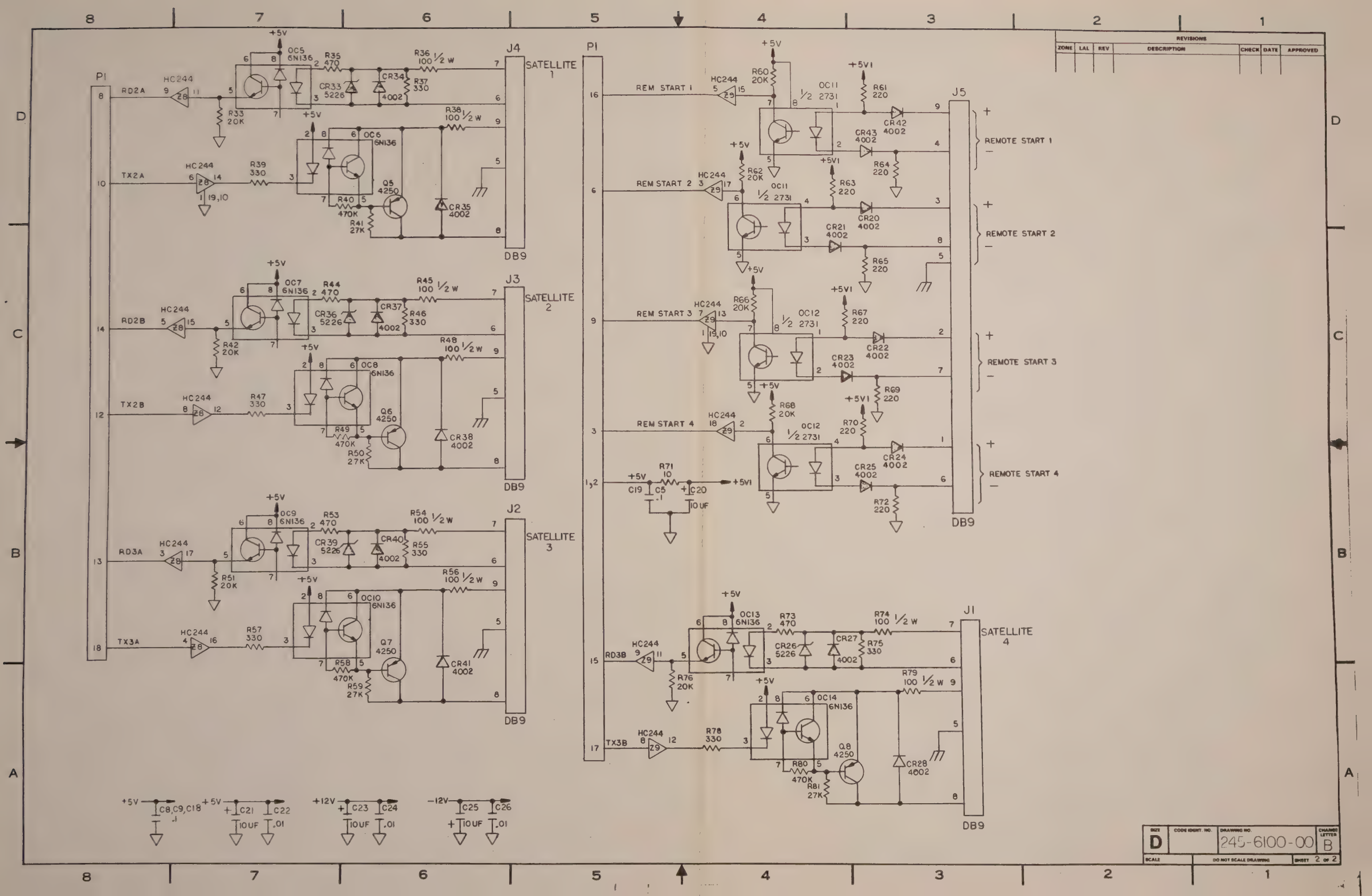
	CHECK	SCALE — · DO NOT SCALE DRAWING · SHEET 1 OF 2	
	APPR.		



P1
RD2A
TX2A
RD2B
TX2B
RD3A
TX3A
RD3B
TX3B
HC244
J4
SATELLITE 1
J3
SATELLITE 2
J2
SATELLITE 3
J1
SATELLITE 4
J5
DB9
REM START 1
REM START 2
REM START 3
REM START 4
REMOTE START 1
REMOTE START 2
REMOTE START 3
REMOTE START 4
+5V
+5V1
+12V
-12V
C8,C9,C18 .1
C21 10UF
C22 .01
C23 10UF
C24 .01
C25 10UF
C26 .01
C19 C5 .1
C20 10UF
REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
SIZE D
CODE IDENT. NO.
DRAWING NO. 245-6100-00
CHANGE LETTER B
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 2

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, INTERFACE		245-4100-00	B
	MODEL NO. 245	DATE 10-27-83	SHEET 3 OF 4

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, INTERFACE	245-2100-00	1	
2	SCHEMATIC, INTERFACE	245-6100-00	1	
3	TEST SPEC			
4				
5				
6	IC, 6N136 OPTO ISO	965-570-09	12	OC1-OC10,OC13, OC14
7	IC, MC1489 GUAD LINE RCVR RS232C	965-601-00	2	Z3,Z5
8	IC, 2731	965-570-05	2	OC11,OC12
9	IC, 74HC00 4-2 IN NAND (TI)	965-6351-00	1	Z1
10	IC, 74HC04 HEX INV (FC,MO,NL)	965-6351-05	2	Z2,Z4
11	IC, DS75150J-8	965-642-00	2	Z6,Z7
12	IC 74HC244	965-6351-03	2	Z8,Z9
13				
14				
15	RES, CARBON 1/4W ±5%, 100	942-201-01	4	R10,R11,R26,R27
16	RES, CARBON 1/4W ±5%, 130	942-201-31	2	R5,R21
17	RES, CARBON 1/4W ±5%, 20K	942-202-03	12	R1,16,17,31,33,42, R51,60,62,66,68,76
18	RES, CARBON 1/4W ±5%, 220	942-202-21	8	R61,R63-65,R67, R69,R70,R72
19	RES, CARBON 1/4W ±5%, 2.2K	942-202-22	4	R4,R12,R20,R28
20	RES, CARBON 1/4W ±5%, 330	942-203-31	12	R2,13,18,29,37,39, R46,47,55,57,75,78
21	RES, CARBON 1/4W ±5%, 33K	942-203-33	6	R7-R9,R23-R25
22	RES, CARBON 1/4W ±5%, 470	942-204-71	4	R35,R44,R53,R73
23	RES, CARBON 1/4W ±5%, 10K	942-201-03	2	R6,R22
24	RES, CARBON 1/4W ±5%, 470K	942-204-74	8	R3,R14,R19,R30,R40, R49,R58,R80

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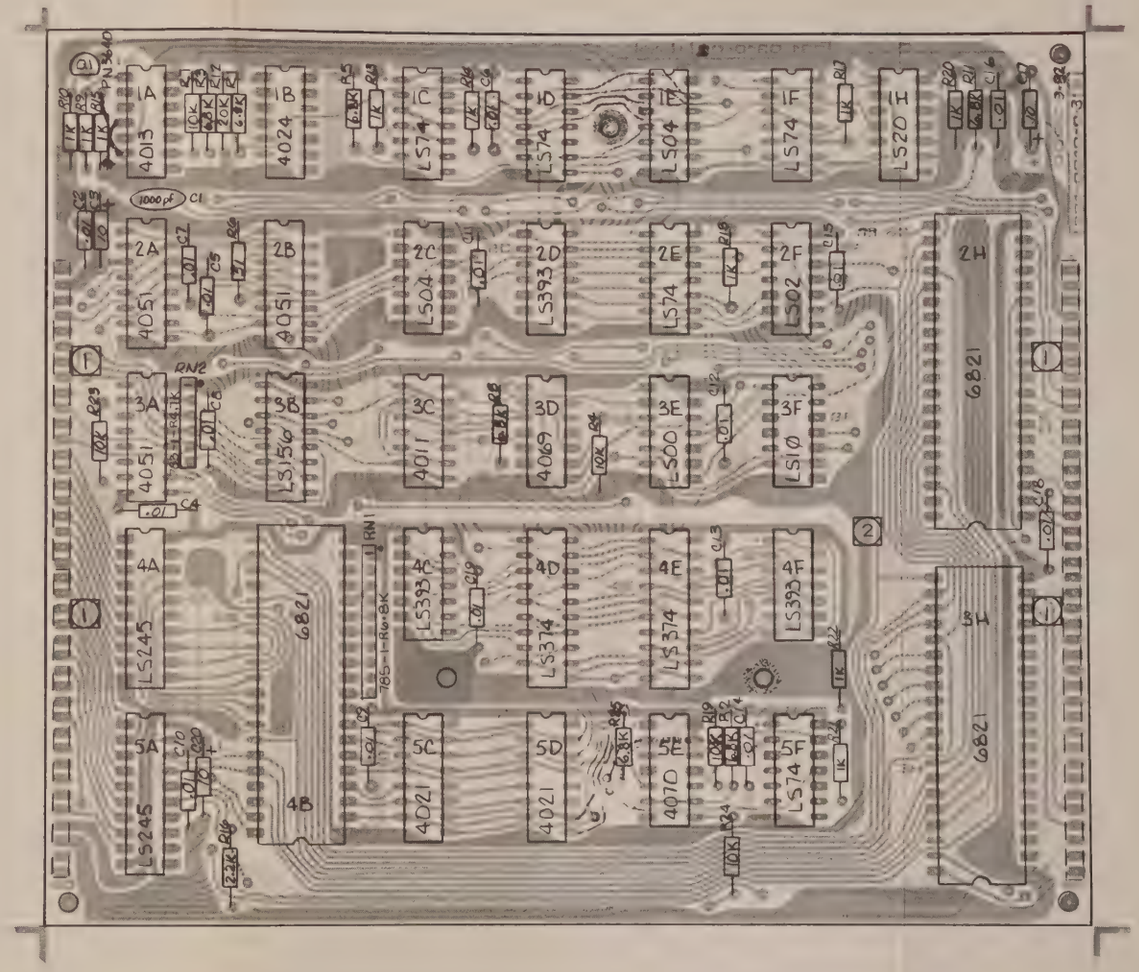
MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
ASSEMBLY PCB, INTERFACE	ML	245-4100-00	B
	MODEL NO. 245	DATE 10-27-83	SHEET 4 OF 4

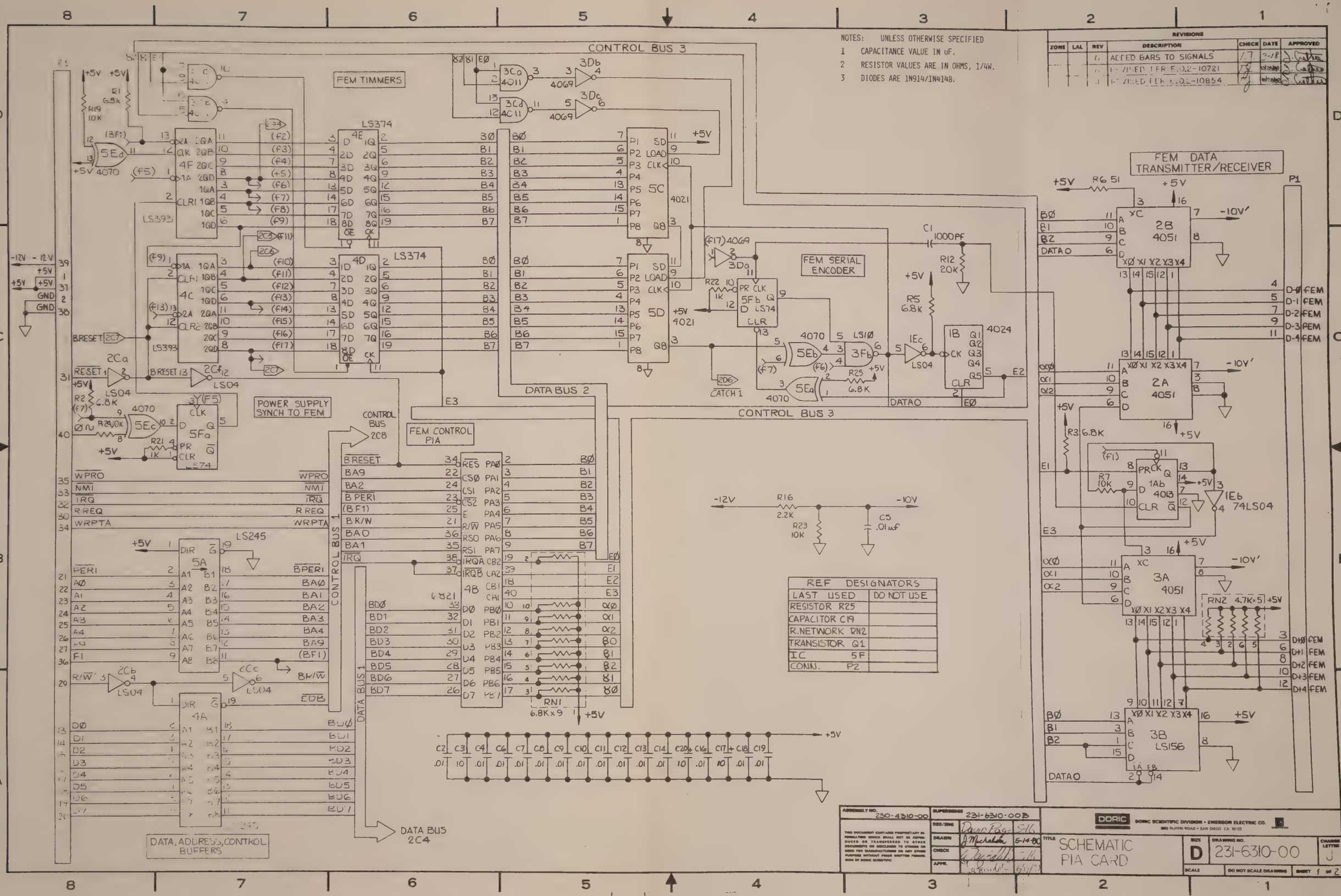
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ±5%, 82	942-208-20	2	R15,R32
26	RES, CARBON 1/2W ±5%, 100	942-301-01	8	R36,R38,R45,R48, R54,R56,R74,R79
27	RES, CARBON 1/4W ±5%, 10	942-201-00	1	R71
28	RES, CARBON 1/4W ±5%, 27K	942-202-73	4	R41,R50,R59,R81
29				
30				
31				
32	CAP, AXIAL .01/50V 180/25V050A	900-021-07	7	C1-C4,C49,C51, C53
33	CAP, .1 @ 50V (VARADYNE 1802)	900-021-08	5	C5,C8,C9, C18,C19
34	CAP, TANT 10 @ 10V (162D)	916-010-10	4	C47,C48,C50,C52
35	JUMPER, J.500X.125T22	991-010-05	2	JMP1-2
36				
37	DIODE, ZENER 1N5226 5.1V	961-522-60	8	CR1,CR3,CR5,CR7, CR26,CR33,CR36,CR39
38	DIODE, 1N4002 100V 1A	966-002-00	32	CR8-25,27-32,34,35, CR37,38,40-43
39				
40				
41	XSTER, 2N4250	962-425-00	8	Q1-Q8
42				
43	SWITCH DPDT 76SD02S (GRAYHILL)	969-050-15	2	S1,S2
44	CONN, 40 PIN	973-0710-00	1	P1
45	CONN, RECPT 25 PIN	973-0101-57	2	J6,J7
46	CONN, RECPT 9 PIN	973-0101-56	5	J1-J5
47				
48	STD-OFF SWAGE 5/16 X 4-40 A2	991-020-36	14	J1-J7



ASSEMBLY

P.C.B. PIA

231-4310-00G



NOTES: UNLESS OTHERWISE SPECIFIED
1 CAPACITANCE VALUE IN uF.
2 RESISTOR VALUES ARE IN OHMS, 1/4W.
3 DIODES ARE 1N914/1N4148.
REVISIONS
ZONE LAL REV DESCRIPTION CHECK DATE APPROVED
ADDED BARS TO SIGNALS
REVISED PER E.O.2-10721
REVISED PER E.O.2-10854
CONTROL BUS 3
FEM TIMMERS
FEM DATA TRANSMITTER/RECEIVER
FEM SERIAL ENCODER
POWER SUPPLY SYNCH TO FEM
FEM CONTROL PIA
DATA BUS 2
CONTROL BUS 1
DATA BUS 1
DATA, ADDRESS, CONTROL BUFFERS
CONTROL BUS 2C8
DATA BUS 2C4
REF DESIGNATORS
LAST USED DO NOT USE
RESISTOR R25
CAPACITOR C19
R.NETWORK RN2
TRANSISTOR Q1
IC 5F
CONN. P2
ASSEMBLY NO. 230-4310-00
SUPERSEDES 231-6310-00B
DORIC
DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
SCHEMATIC PIA CARD
D 231-6310-00
SHEET 1 OF 2

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

IC POWER DISTRIBUTION TABLE

REF DESIG	IC TYPE	POWER		
		+5V	GND	-10V*
5A 4A	74LS245	20	10	—
4B 2H 3H	6821	20	1	—
1A	4013	14	7	—
2E,5F,1F,1C,1D	74LS74	14	7	—
3E	74LS00	14	7	—
2F	74LS02	14	7	—
2D, 4C, 4F	74LS393	14	7	—
3F	74LS10	14	7	—
5E	4070	14	7	—
4E, 4D	74LS374	20	10	—
5C, 5D	4021	16	8	—
3C	4011	14	7	—
2C, 1E	74LS04	14	7	—
1H	74LS20	14	7	—
3B	74LS156	16	8	—
2A 2B 3A	4051	16	8	7
1B	4024	14	7	—

ASSEMBLY NO.	SUPERSEDES			
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	DRAWN	PHERRON	4-80	
	CHECK			
	APPR.		6/1/	

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TITLE: SCHEMATIC PIA CARD

SIZE	DRAWING NO.	CHANGE LETTER
D	231-6310-00	J

SCALE — DO NOT SCALE DRAWING — SHEET 2 OF 2

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, PIA BOARD	MODEL NO. 235	231-4310-00	G
		DATE 4-15-79	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, PIA BOARD	231-2310-03	1	
2	SCHEMATIC	231-6310-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 4011 4-2IN NAND CMOS(MO)	965-587-02	1	3C
7	IC, 74C04(4069)HEX INV CMOS(RC)	965-587-05	1	3D
8	IC, 4024 7-ST BIN CNTR CMOS(FC)	965-587-22	1	1B
9	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	1A
10	IC, 4070 4-EXCL OR CMOS (FC)	965-565-05	1	5E
11	IC, 4021 8STG SR(FC,NL,MO)	965-587-43	2	5C,5D
12	IC, 6821 PIA (MO,FC)	965-613-10	3	2H,4B,3H
13	IC, 74LS04 HEX INV(FC,MO,NL)	965-635-00	2	1E,2C
14	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	2	4A,5A
15	IC, 74LS374J 8 3-ST REG(AMD,F)	965-635-05	2	4D,4E
16	IC, 74LS393 DUAL 4BIN CTR(FC,TI	965-635-06	3	2D,4C,4F
17	IC, 74LS00 4-2IN NAND (TI)	965-635-07	1	3E
18	IC, 74LS10 3-3IN NAND (TI)	965-635-08	1	3F
19	IC, 74LS02 QUAD 2 IN NOR	965-635-17	1	2F
20	IC, 74LS74 DUAL D F/F	965-635-19	5	1C,1D,1F,2E,5F
21	IC,74LS20 DUAL 4-IN POSNAND	965-635-35	1	1H
22	IC, 74LS156	965-635-48	1	3B
23				
24				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, PIA BOARD	MODEL NO. 235	DATE 4-15-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26				
27				
28				
29	RES, CARBON 1/4W ±5%, 2.2K	942-202-22	1	R16
30				
31	RES, CARBON 1/4W ± 5%, 1K	942-201-02	10	R9-10,R13-15, R17-18,R20-22
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	5	R19 R4,R7,R24,R23
33	RES, CARBON 1/4W ± 5%, 20K	942-202-03	1	R12
34	RES, CARBON 1/4W ± 5%, 6.8K	942-206-82	7	R1,R2,R5,R8,R11 R3,R25
35	RES NTWK 6.8K SIP(785-1-R6.8K)	950-068-01	1	RN1
36	RES, CARBON 1/4W ± 5%, 51Ω	942-205-10	1	R6
37	RES NTWK 4.7K SIP(783-1-R4.7K)	953-047-01	1	RN2
38				
39				
40				
41				
42	CAP,AXIAL .01/50V 180/Z5V050A	900-021-07	16	C2,C4-16,C18, C19
43	CAP, MICA, .001	915-031-02	1	C1
44	CAP, 10uf, TANT 10V (162D)	916-010-10	3	C3,C17,C20
45				
46				
47				
48				

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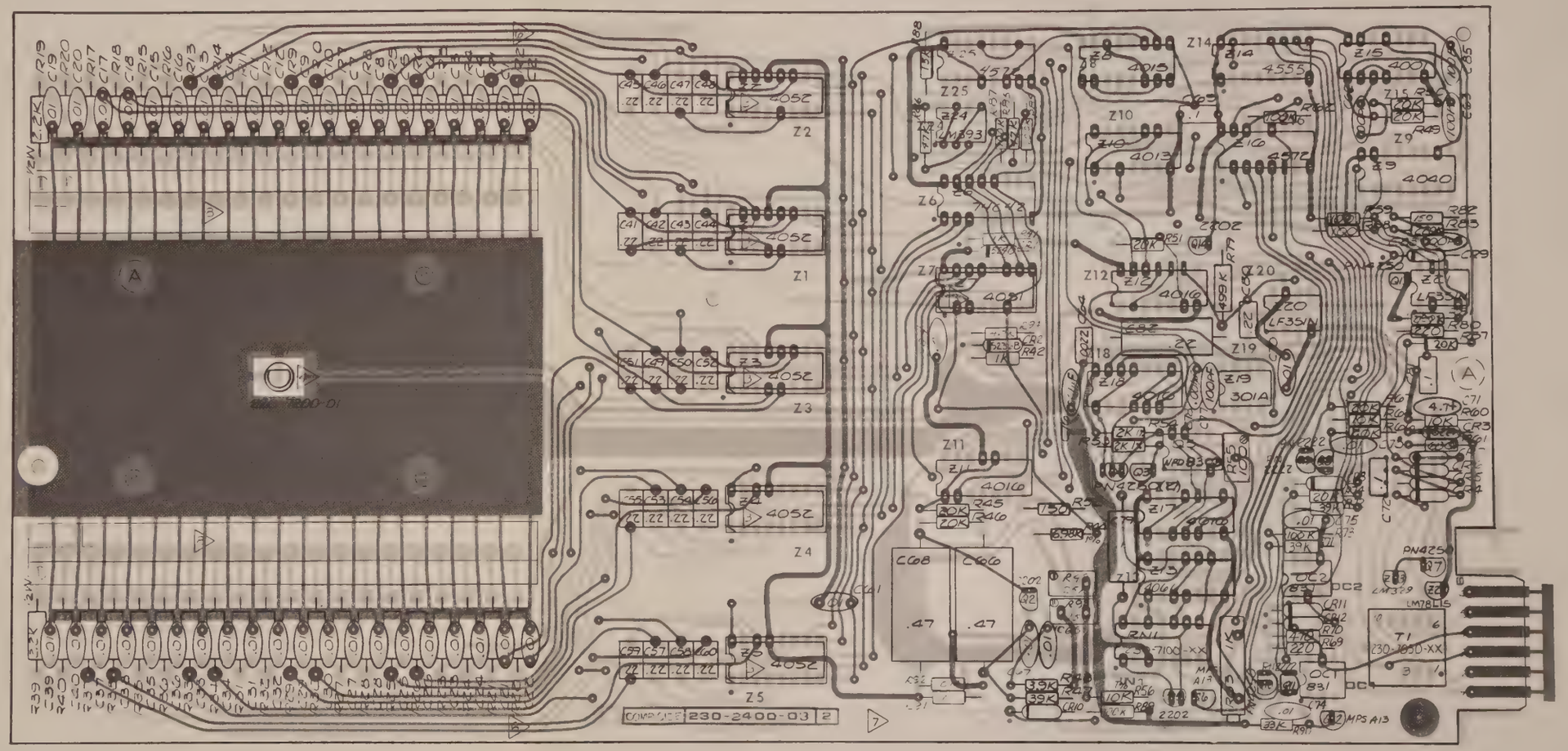
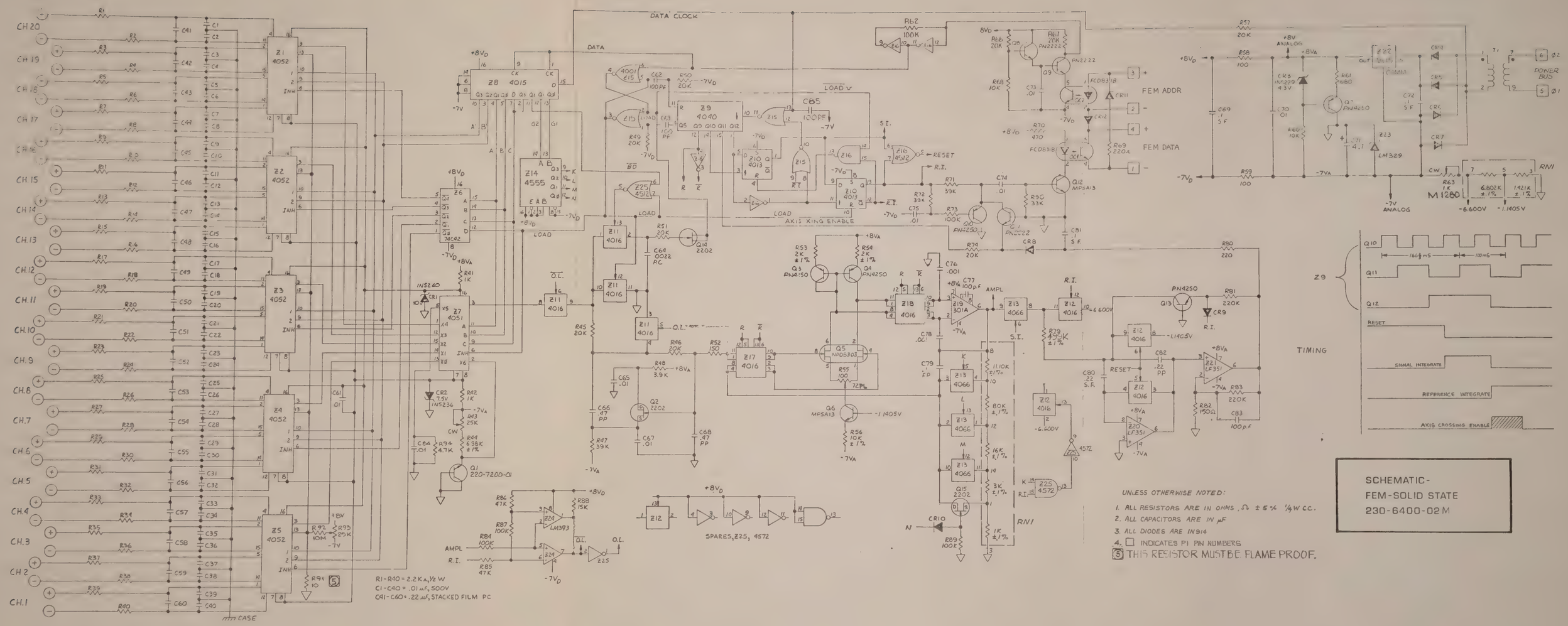
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, PIA BOARD		231-4310-00	G
	MODEL NO. 235	DATE 4-15-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50	SELEC TED 4051 CMOS MULTI	000-8050-00	3	2A,2B,3A
51	XSTR, 2N3640 (PNP)(FC,NL)	962-364-00	1	Q1
52	CONN, PC20M (MOLEX 22-10-2201)	973-0101-12	4	P1,P2



ASSEMBLY
SOLID STATE FEM
230-4400-03C


DATA CLOCK
DATA
LOAD
AXIS XING ENABLE
FEM ADDR
FEM DATA
POWER BUS
TIMING
SIGNAL INTEGRATE
REFERENCE INTEGRATE
AXIS CROSSING ENABLE
SPARES, Z25, 4572
CASE
R1-R40 = 2.2 K Ω, 1/2 W
C1-C40 = .01 μf, 500V
C41-C60 = .22 μf, STACKED FILM PC
UNLESS OTHERWISE NOTED:
1. ALL RESISTORS ARE IN OHMS, Ω ± 5% 1/4 W CC.
2. ALL CAPACITORS ARE IN μF
3. ALL DIODES ARE IN914
4. ☐ INDICATES P1 PIN NUMBERS
5 THIS RESISTOR MUST BE FLAME PROOF.
SCHEMATIC-
FEM-SOLID STATE
230-6400-02 M

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY SOLID STATE FEM	MODEL NO. 235	230-4400-03	C
		DATE 3-18-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB SOLID STATE FEM	230-2400-03	1	
2	SCHEMATIC	230-6400-02	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COM(8DIP)(NL)	965-580-00	1	Z24
7	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z15
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z8
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z10
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z6
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z9
13	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
14	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z19
15	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z20,Z21
16	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z16,Z25
17	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z23
18	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z22
19				
20				
21				
22				
23				
24	RES, FILM RN60C 1% 499K	920-449-93	1	R79

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY SOLID STATE FEM	MODEL NO. 235	230-4400-03	C
		DATE 3-18-80	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D 1% 10K	924-310-02	1	R56
26	RES, FILM RN55C 1% 2K	924-420-01	2	R53,R54
27	RES, FILM RN55C 1% 6.98K	924-469-81	1	R44
28	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	1	R91
29	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R58,R59
30	RES, CARBON 1/4W ± 5%, 1K	942-201-02	2	R41,R42
31	RES, CARBON 1/4W ± 5%, 10K	942-201-03	2	R60,R68
32	RES, CARBON 1/4W ± 5%, 100K	942-201-04	5	R62,73,84,87 & 89
33	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
34	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R88
35	RES, CARBON 1/4W ± 5%, 10M	942-201-06	1	R92
36	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
37	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R69,R80
38	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
39	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R90
40	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
41	RES, CARBON 1/4W ± 5%, 39K	942-203-93	3	R47,R71,R72
42	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
43	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R94
44	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R85,R86
45	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61
46	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	40	R1-R40
47				
48				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE FEM	MODEL NO. 235	230-4400-03	C
	DATE 3-18-80	SHEET 5 OF 6	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51	CAP, TANT. 4.7 @ 35V (1960)	916-470-35	1	C71
52	CAP, DISC .01/500V (5GA)	900-021-04	48	C1-40,C61,C65,67, C70, ,73-75,84
53	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
54	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	5	C62,63,77,83,85
55	CAP,PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
56	CAP,PLP,.22/200V,IMB(GA2C224K)	917-022-20	1	C82
57	CAP,PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,68
58	CAP, SF, .1/100V, SMS(B32570)	918-001-10	3	C69,72,81
59	CAP, SF, .0022/250V, SMS(32570)	918-002-25	1	C64
60	CAP, SF, .22/100V, SMS(B32570)	918-022-10	21	C41-60,C80
61				
62				
63				
64				
65				
66	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	9	CR4-12
67	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
68	DIODE, 1N5236B (7.5V)	961-523-62	1	CR2
69				
70	DIODE, 1N5240, 10V	961-524-00	1	CR1
71				
72				

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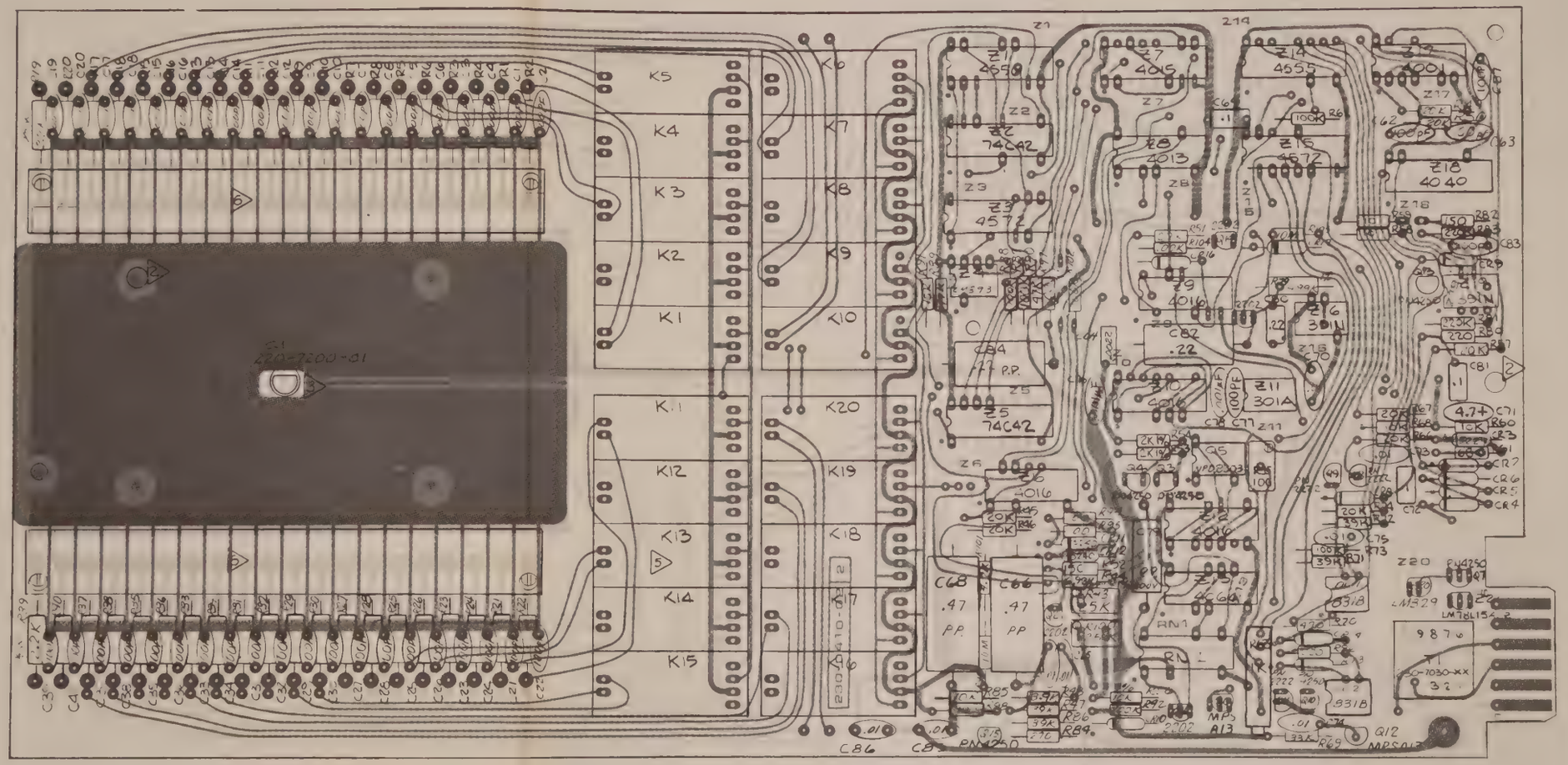
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE FEM	MODEL NO. 235	DATE 3-18-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76	GRADED 4016	000-7700-00	4	Z11,Z12,Z17,Z18
77	SELECTED 4051 CMOS MULTI	000-8050-00	1	Z7
78	SELECTED 4052 CMOS MULTI	000-8051-00	5	Z1-5
79	FET, 2202 (NJ,LO-LK,GP)	100-722-02	3	Q2,Q14,Q15
80	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
84	POT, 100 CERMET (72PL)	960-015-19	1	R55
85	POT, 25K MT2X253	960-015-15	2	R43,R93
86	XSTR. PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
87	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	5	Q3,Q4,Q7,Q10, Q13
88	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Q5
89	XSTR, MPSA13 (NPNA/DRL92) (M)	964-040-03	2	Q6,Q12
90	OPTO, FCD831B (FC)	965-570-03	2	OC1,OC2
91	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
92	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
93	IC SOCKET, 16DIP PC (316AG5DR)	992-010-22	6	
94	DISS-O-PAD .250 O.D. X .125 I.D. X .03 Bivar Inc. TO-16-03	979-020-11	6	


K5
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4698
Z2
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Z3
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74C42
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4015
Z8
4013
Z9
4016
Z10
4016
Z11
301A
Z12
4555
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4572
Z14
4001
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4572
Z16
3011
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Z18
4040
Z19
Z20
LM329
LM78L15
C1
220-7200-01
C82
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C84
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C101
.01
C102
.01
C103
.01
C104
.01
C105
.01
C106
.01
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.01
C108
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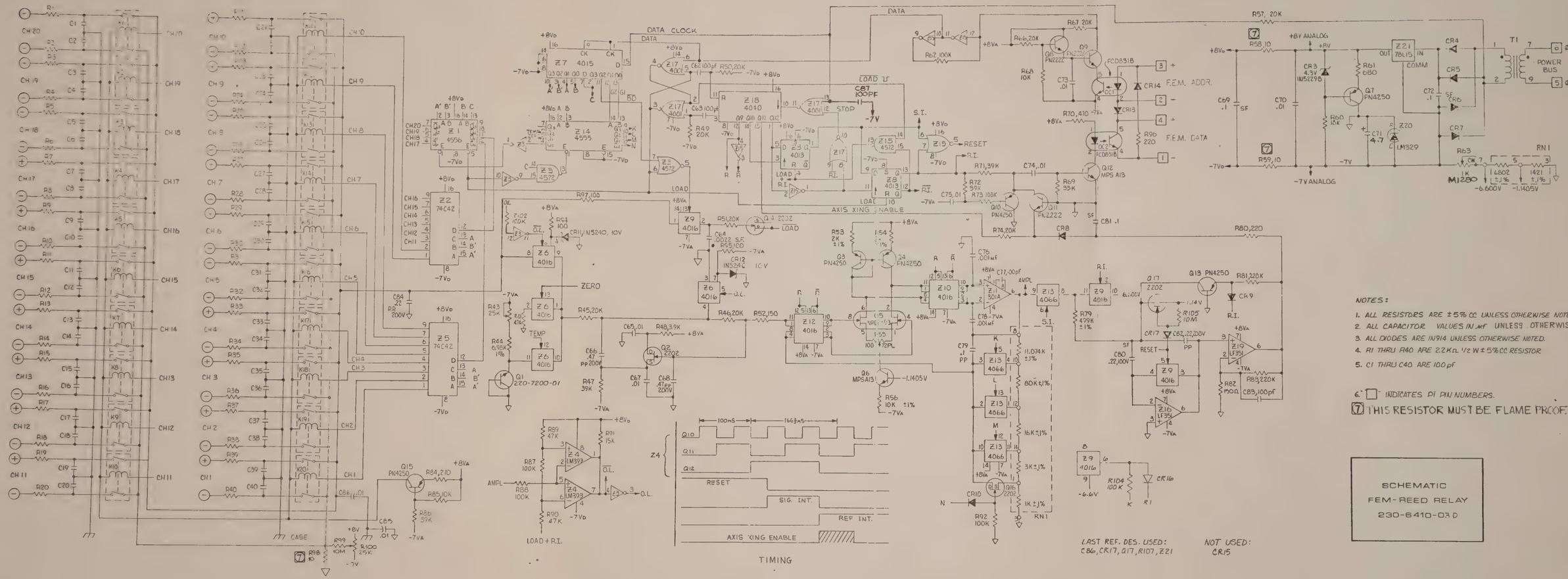

NOTES:

1. ALL RESISTORS ARE ±5% CC UNLESS OTHERWISE NOTED.
2. ALL CAPACITOR VALUES IN mf UNLESS OTHERWISE NOTED.
3. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED.
4. R1 THRU R40 ARE 2.2KΩ 1/2 W ± 5% CC RESISTOR
5. C1 THRU C40 ARE 100 pf
6. □ INDICATES PI PIN NUMBERS.
7. THIS RESISTOR MUST BE FLAME PROOF.

LAST REF. DES. USED: C86, CR17, Q17, R107, Z21

NOT USED: CR15

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	F
		DATE 3-17-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB REED FEM	230-2410-02	1	
2	SCHEMATIC	230-6410-03	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
7	IC, 4001 4-2IN NOR CMOS(MO)	965-587-01	1	Z17
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z7
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	Z8
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	2	Z2,Z5
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z18
13	IC, 4556 DUAL 10F4 DEC(MO,FC,NL	965-587-48	1	Z1
14	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
15	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z11
16	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z16,Z19
17	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z3,Z15
18	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z20
19	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z21
20				
21				
22				
23				
24				

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	F
		DATE 3-17-89	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C, 499K	920-449-93	1	R79
26	RES, FILM RN55D 1% 10K	924-310-02	1	R56
27	RES, FILM RN55C 2K	924-420-01	2	R53-54
28	RES, FILM RN55C 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	3	R58,R59,R98
30	RES, CARBON 1/4W ± 5%, 100	942-201-01	3	R94,R95,R97
31				
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	3	R60,R68,R85
33	RES, CARBON 1/4W ± 5%, 100K	942-201-04	7	R62,R73,R87-88 R92,R102,R104
34	RES, CARBON 1/4W ± 5%, 10M	942-201-06	2	R99,R105
35				
36	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
37	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R91
38	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
39	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R96
40	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
41	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R84
42	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69
43	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
44	RES, CARBON 1/4W ± 5%, 39K	942-203-93	4	R47,R71-72,R86
45	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
46	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R101
47	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R89,R90
48	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	F
		DATE 3-17-80	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	40	R1-40
50				
51				
52				
53				
54	CAP, TANT, 4.7 @ 35V (1960)	916-470-35	1	C71
55	CAP, DISC .01/500V (5GA)	900-021-04	8	C65,C67,C70, C73-75,C85-86
56	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
57	CAP, DISC, 100 PF @ 1 KV (5GA)	901-011-01	45	C1-40,C62-63, C77,C83,C87
58	CAP, PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
59	CAP, PLP,.22/200V,IMB(GA2C224K)	917-022-20	2	C82,C84
60	CAP, PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
61	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C69,C72,C81
62	CAP, SF, .0022/250V, SMS(B32570)	918-002-25	1	C64
63	CAP,SF, .22/100V, SMS (B32570)	918-022-10	1	C80
64				
65				
66				
67				
68				
69	DIODE, 1N914 (1N4148)(RD,FC,TI	961-091-40	11	CR4-10,CR13, CR14,CR16,CR17
70	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
71				
72	DIODE, IN5240, 10V	961-524-00	2	CR11,CR12

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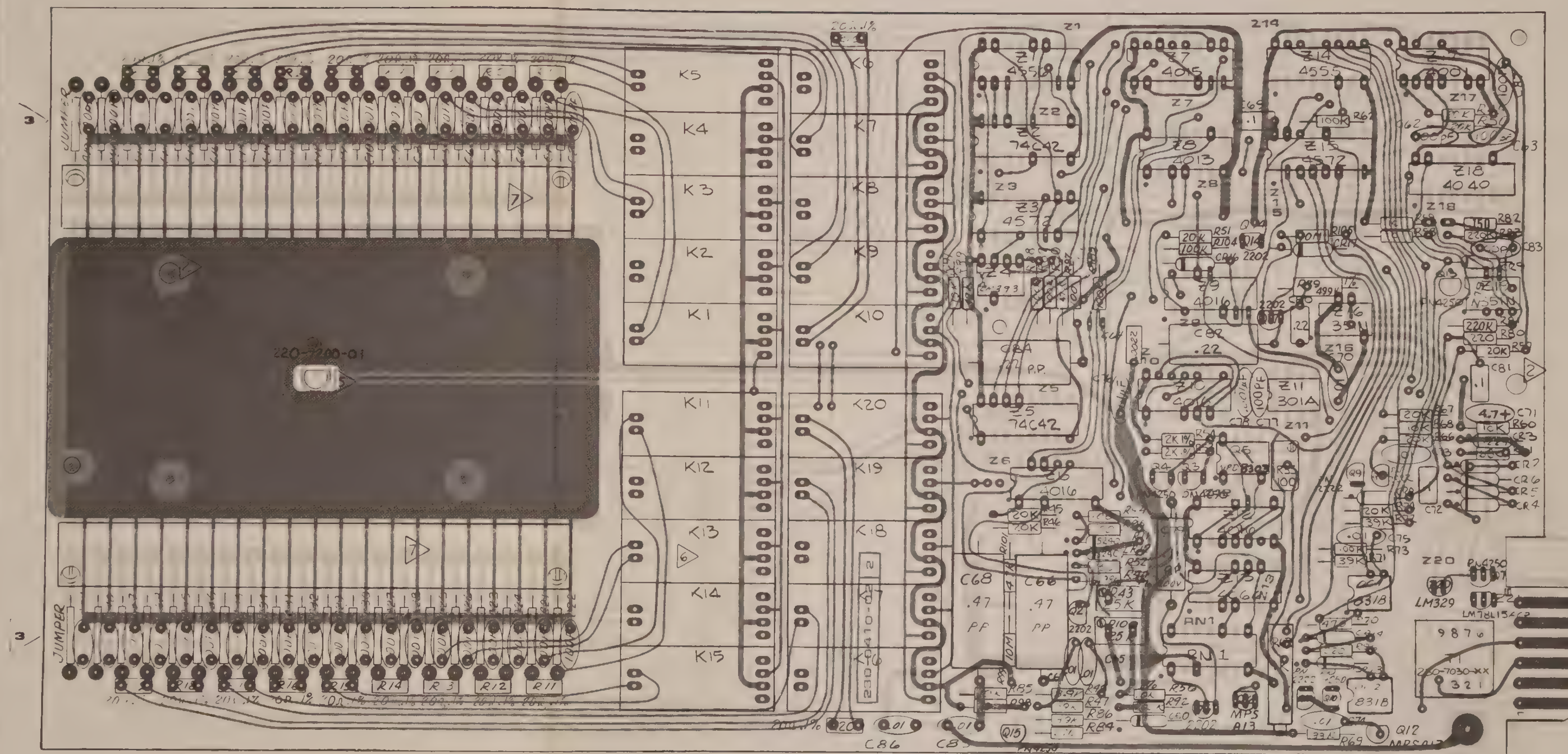
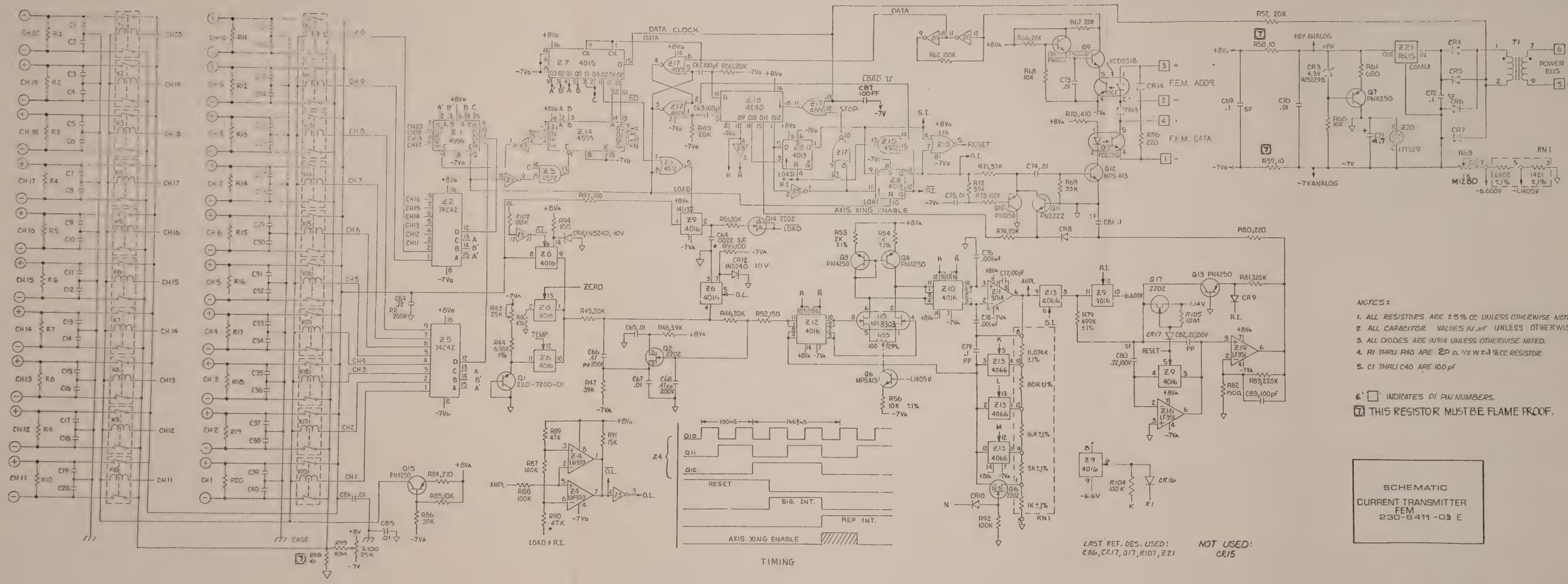
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	F
	DATE 3-17-80	SHEET 6 OF 6	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
78	GRADED 4016	000-7700-00	4	Z6,Z9-10,Z12
79	RELAY, REED LOW THERMAL	000-8043-00	20	K1-20
80	FET, 2202 (NJ,LO-LK,GP)	100-722-02	4	Q14,Q16,Q17,Q2
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
83	POT, 100 CERMET (72PL)	960-015-19	1	R55
84	POT, 25K MT2X253	960-015-15	2	R43,R100
85	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
86	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	6	Q3-4,Q7,Q10, Q13,Q15
87	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Q5
88	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
89	OPTO, FCD8316 (FC)	965-570-03	2	OC1,OC2
90	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
91	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
92	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	6	



ASSEMBLY
CURRENT TRANSMITTER FEM
230-4411-03F



NOTES:

1. ALL RESISTORS ARE ±5% CC UNLESS OTHERWISE NOTED.
2. ALL CAPACITOR VALUES IN μf UNLESS OTHERWISE NOTED.
3. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED.
4. R1 THRU R40 ARE 20 Ω 1/2 W ±.1% CC RESISTOR
5. C1 THRU C40 ARE 100 pf
6. ☐ INDICATES PI PIN NUMBERS.
7. THIS RESISTOR MUST BE FLAME PROOF.

LAST REF. DES. USED: C86, CR17, Q17, R107, Z21

NOT USED: CR15

SCHEMATIC
CURRENT TRANSMITTER
FEM
230-6411-03 E

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XMTR	MODEL NO. 235	DATE 3-17-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB REED FEM	230-2410-02	1	
2	SCHEMATIC	230-6411-03	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
7	IC, 4001 4-2IN NOR CMOS(MO)	965-587-01	1	Z17
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z7
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	Z8
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	2	Z2,Z5
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z18
13	IC, 4556 DUAL 10F4 DEC(MO,FC,NL	965-587-48	1	Z1
14	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
15	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z11
16	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z16,Z19
17	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z3,Z15
18	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z20
19	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z21
20				
21				
22				
23				
24				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XMTR.	MODEL NO. 235	DATE 3-17-89	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C, 499K	920-449-93	1	R79
26	RES, FILM RN55D 1% 10K	924-310-02	1	R56
27	RES, FILM RN55C 2K	924-420-01	2	R53,R54
28	RES, FILM RN55C 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	3	R58,R59,R98
30	RES, CARBON 1/4W ± 5%, 100	942-201-01	3	R94,R95,R97
31				
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	3	R60,R68,R85
33	RES, CARBON 1/4W ± 5%, 100K	942-201-04	7	R62,R73,R87-88, R92,R102,R104
34	RES, CARBON 1/4W ± 5%, 10M	942-201-06	2	R99,R105
35				
36	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
37	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R91
38	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
39	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R96
40	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
41	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R84
42	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69
43	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
44	RES, CARBON 1/4W ± 5%, 39K	942-203-93	4	R47,R71-72,R86
45	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
46	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R101
47	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R89,R90
48	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XMTR.	MODEL NO. 235	230-4411-03	F
		DATE 3-17-80	SHEET 5 OF 6

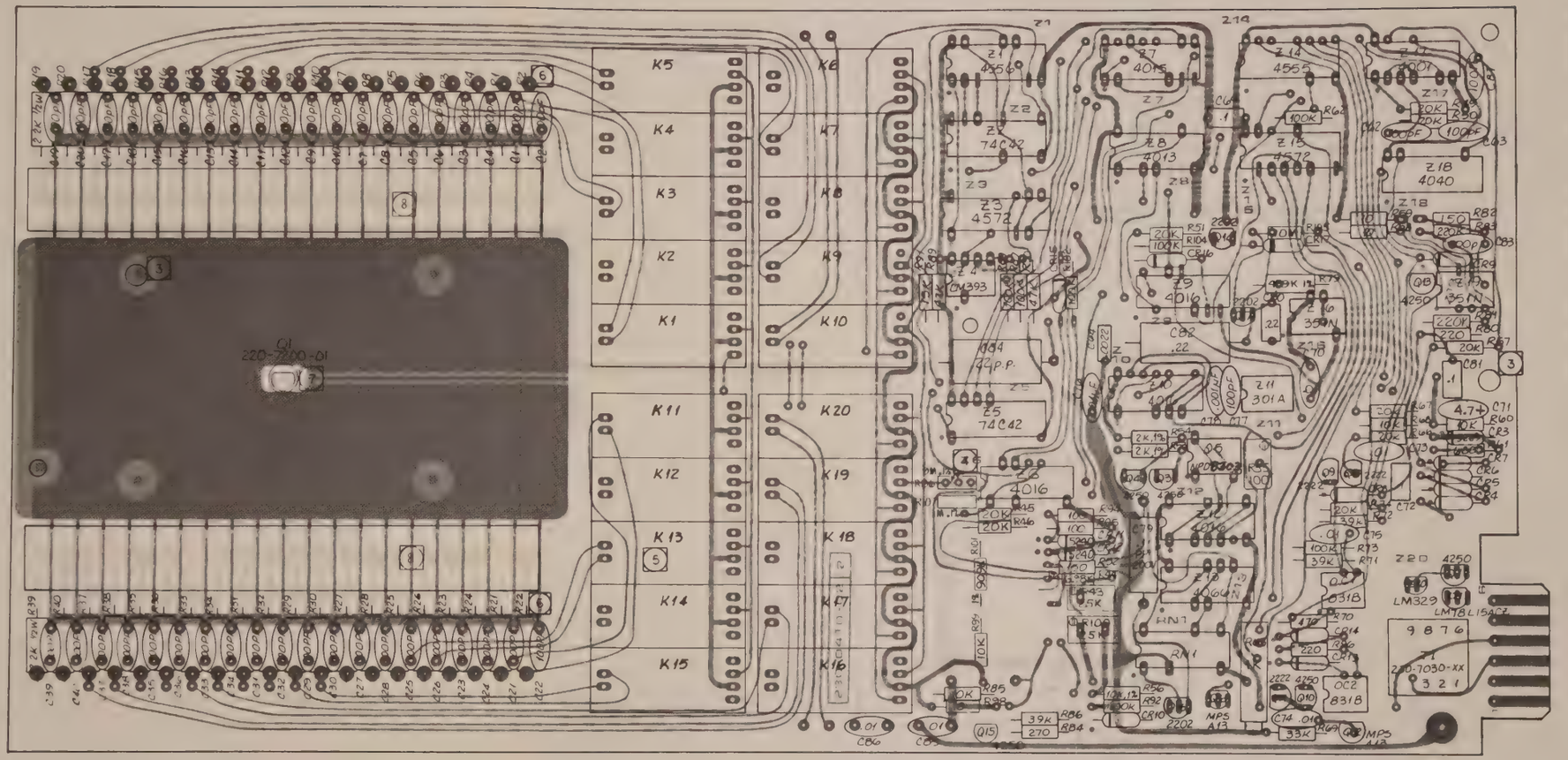
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, WW, .1%, 20	938-002-00	20	R1-20
50				
51				
52				
53				
54	CAP, TANT 4.7 @ 35V (1960)	916-470-35	1	C71
55	CAP, DISC .01/500V (5GA)	900-021-04	8	C65,C67,C70, C73-75,C85-86
56	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
57	CAP, DISC, 100 PF @ 1 KV (5GA)	901-011-01	45	C1-40,C62-63, C77,C83,C87
58	CAP, PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
59	CAP, PLP,.22/200V,IMB(GA2C224K)	917-022-20	2	C82,C84
60	CAP, PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
61	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C69,C72,C81
62	CAP, SF, .0022/250V, SMS(B32570)	918-002-25	1	C64
63	CAP,SF, .22/100V, SMS(B32570)	918-022-10	1	C80
64				
65				
66				
67				
68				
69	DIODE, 1N914 (1N4148)(RD,FC,TI	961-091-40	11	CR4-10,CR13, CR14,CR16,CR17
70	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
72	DIODE, IN5240, 10V	961-524-00	2	CR11,CR12

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XTRM.	MODEL NO. 235	230-4411-03	F
		DATE 3-17-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
78	GRADED 4016	000-7700-00	4	Z6,Z9,Z10,Z12
79	RELAY, REED LOW THERMAL	000-8043-00	20	K1-20
80	FET, 2202 (NJ,LO-LK,GP)	100-722-02	4	Q14,Q16-17,Q2
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
83	POT, 100 CERMET (72PL)	960-015-19	1	R55
84	POT, 25K MT2X253	960-015-15	2	R43,R100
85	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
86	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	6	Q3-4,Q7,Q10,Q13 Q15
87	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Q5
88	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
89	OPTO, FCD8316 (FC)	965-570-03	2	OC1,OC2
90	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
91	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
92	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	6	
93	JUMPER J.600 X .125 T22	991-010-06	1	



ASSEMBLY-
HIGH VOLTAGE
230-4412-02V

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MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
ASSEMBLY, PCB, LOW POWER RTD FEM	ML	231-4601-01	B
	MODEL NO. 235	DATE 6-14-83	SHEET 5 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	CAP, SF, .1/100V, SMS (B32570)	918-001-10	1	C72
50	RES, CARBON 1/4W ± 5%, 47K	942-204-73	3	R93,R97,R101
51	RES, CARBON 1/4W ± 5%, 51	942-205-10	1	R168
52	RES, CARBON 1/4W ± 5%, 680K	942-206-84	1	R84
53	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	100	R1-R40,R104-R163
54	RES, CARBON 1/4W ± 5%, 470K	942-204-74	3	R94,R96,R99
55	RES, CARBON 1/4W ± 5%, 1M	942-201-05	2	R83,R174
56	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	2	R170,R183
57	RES, CARBON 1/4W ± 5%, 56K	942-205-63	1	R95
58	RES, CARBON 1/4W ± 5%, 10	942-201-00	1	R171
59	CAP, AXIAL .010 @ 50V (5GA)	900-021-07	7	C61,C65,C67, C70,C71,C81,C86
60	CAP, AXIAL .001 @ 50V (5GA)	900-021-09	4	C74-C76, C78
61	CAP, DISC, 100pf @ 1KV (5GA)	901-011-01	5	C62,C63,C77,C84 C88
62	CAP, PLP, .1/200V, IMB(GA2C104K)	917-001-20	1	C79
63	CAP, PLP, .22/200V,IBM(GA2C224K)	917-022-20	1	C82
64	CAP, PLP, .47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
65	CAP, .1µF 50V (VARADYNE 1802)	900-021-08	4	C69, C73,C80, C87
66	CAP, CER., .0022, 50VDC	900-021-12	1	C64
67	CAP, SF, .22/100V, SMS (B32570)	918-022-10	20	C41-C60
68	CAP, DISC, 22pf @ 1KV	901-012-20	1	C85
69	DIODE, 1N5235B (6.8V) (MO)	961-5235-68	1	CR21
70	DIODE, 1N5240B 10V (MO)	961-524-00	1	CR20
71	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	13	CR4-13, CR15, CR16,CR22
72	DIODE, 1N5232B 5.6V (MO)	961-523-22	1	CR3

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, LOW POWER RTD FEM	MODEL NO. 235	231-4601-01	B
		DATE 6-14-83	SHEET 6 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	DIODE, 1N5236B (7.5V)	961-523-62	2	CR2,CR23
74	DIODE, 1N5237B 6.2V (MO)	961-523-72	1	CR1
75	DIODE, LM329 PERCISION 6.9V REF	965-636-00	1	CR14
76	POT, 10K CERMET (66PR10K)	960-0110-39	1	R180
77	POT, 1M CERMET (66PR1M)	960-0110-40	2	R166,R173
78	IC, GRADED 4016	000-7700-00	4	Z23,Z24,Z29,Z30
79	IC, SELECTED 4052 CMOS MULTI	000-8051-00	16	Z1-Z15,Z20
80	XSTR, FET, 2202 (NJ,L)(LK,GP)	100-722-02	2	Q2,Q14
81	XFMR. RTD INTERFACE	230-7060-00	1	T1
82				
83	POT, 1K CERMET (66PR1K)	960-0110-38	3	R55,R88,R167
84				
85				
86	XSTR, PN2222 (NPNA92)(NA)	962-222-20	5	Q1,Q8,Q11,Q17,Q20
87	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	8	Q3,Q4,Q10,Q13, Q15,Q16,Q18,Q19
88	XSTR, FET NPD8303 DUAL N CHANNEL	962-8303-00	1	Q5
89	XSTR, MPSA13 (NPNA/DRL92) (M)	964-040-03	2	Q6,Q12
90	DIODE, LM385Z	961-385-00	1	CR24
91				
92	STDF, 7/16X440 A2 (L6911-10-2A)	991-020-76	4	
93	SPACER, 1/8X6A2 (L6310-2-2A)	991-020-88	3	
94				
95				
96	WASHER, SPLITLOCK #4	986-200-04	4	

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, LOW POWER RTD FEM		231-4601-01	B
	MODEL NO. 235	DATE 6-14-83	SHEET 7 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	WASHER, FLAT #4	986-100-04	4	
98	SCREW, PAN HD, PHILLIPS, 4-40 X 5/16 LG	980-440-031	4	
99	DISS-O-PAD .205 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	12	
100	OPTO, 4N36 (GE) (MOT)	965-5700-11	2	OC1, OC2
101	CONN, 24 POS FEM SOCKET	973-3600-24	1	
102	CONN, 24 PIN STRAIGHT PIN HEADER	973-0101-52	1	
103				
104	TERMINAL STRIP, 10 PIN	973-0101-51	8	
105				
106	SHIELD, LOW POWER RTD FEM	231-2450-00	1	
107				
108				
109				
110				

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A	LIMITED USAGE RELEASE			
		B	REVISED PER E.O.2-10840	DBC		
		C	REVISED PER E.O.2-10053	DBC	6/3/82	
		D	REVISED PER E.O.2-11015	DBC	6/3/82	
		B	REVISED PER E.O.2-11073	KCA	4-14-83	
		C	REVISED PER E.O.2-11193	KCA	4-14-83	
		D	REVISED PER E.O.2-11220	DBC	5/12/83	

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.
2. INSTALL HARDWARE PER CHART.

HARDWARE INSTALLATION CHART			
SYM	QTY	PART NUMBER	REMARKS
A	2	991-020-88	SPACER, FARSIDE

3. INSTALL 16 PIN SOCKET.
4. COMP HEIGHT NOT TO EXCEED 5/16 INCH FROM BOARD.
5. ALL DIODES ARE 1N914.

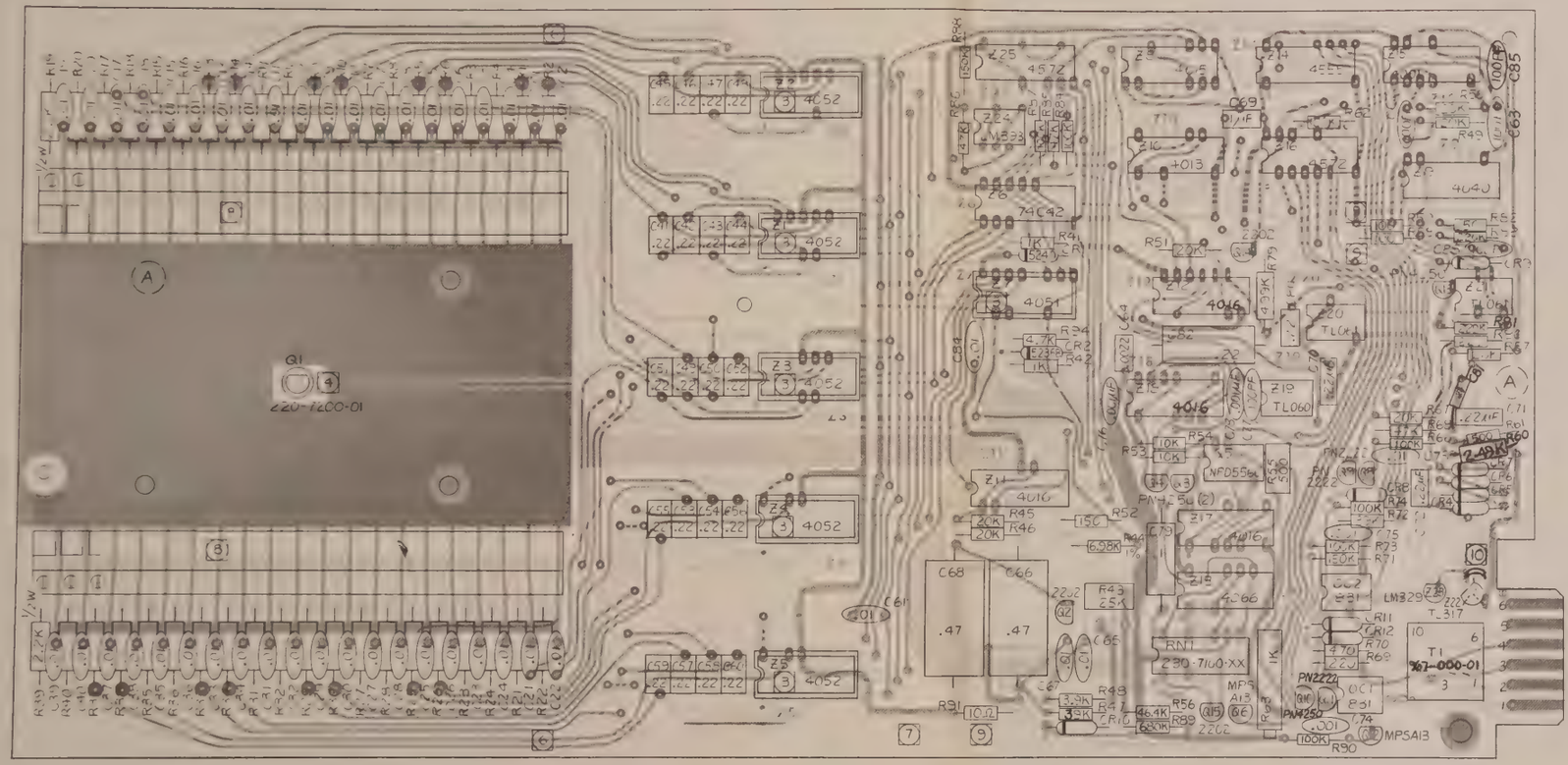
(6) R1 THRU R40 ARE 2.2K, 1/2 W C.C.

(7) RUBBER STAMP ASSY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR (CIRCUIT) SIDE.

(8) INSTALL 3 DISS-O-PADS (TO 16-03) UNDER TERM STRIP, ONE IN CENTER AND ONE ON EACH END.

(9) R58, R59, AND R91 MUST BE FLAMEPROOF.

(10) INSTALL SOLID 24 AWG. TEFLON INSULATED BUS WIRE.



CONTROLLED DOCUMENT

PRIOR NOTIFICATION MUST BE MADE TO FACTORY MUTUAL SYSTEMS BEFORE ANY CHANGES ARE MADE TO THIS DOCUMENT.

ASSEMBLY NO	SUPERSEDES		
	DES-ENG	R Price	8-21-81
	DRAWN	H. LAM	8-10-81
	CHECK	R Price	8-21-81
	APPR	[illegible]	

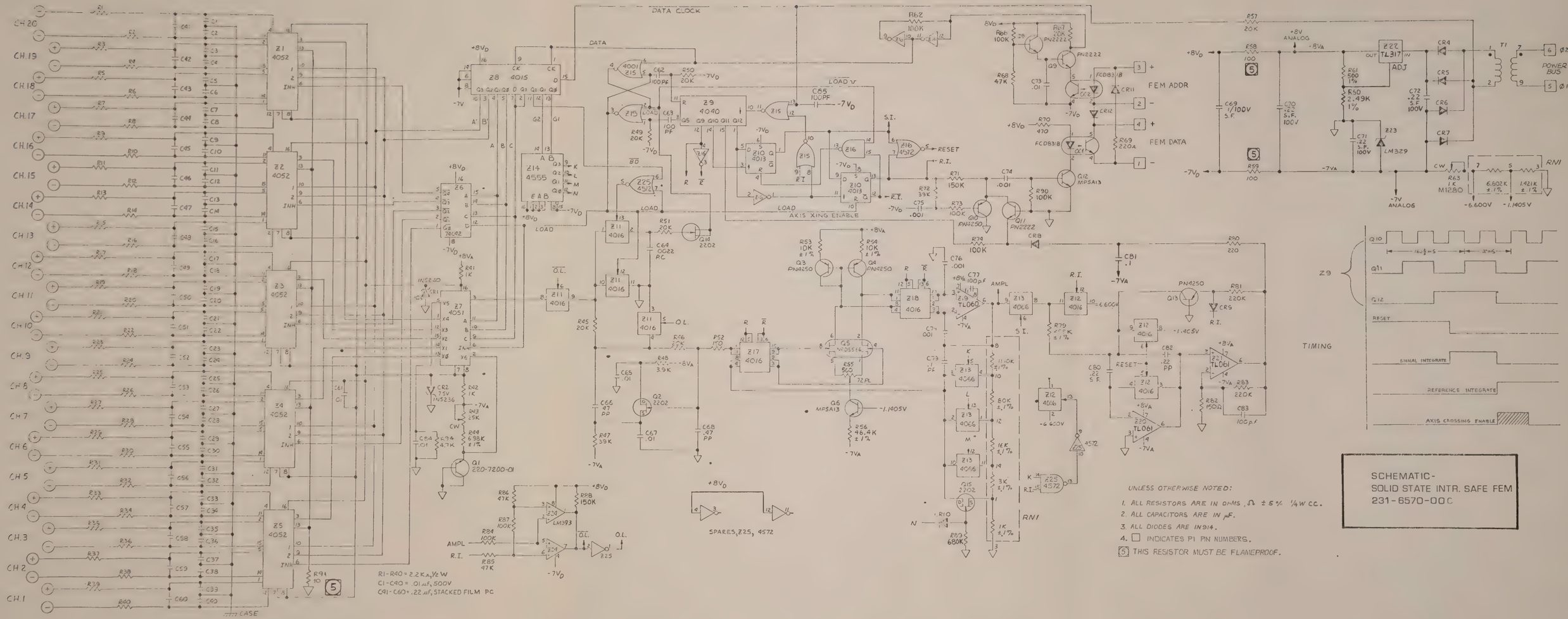
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC.

DORIC DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
2807 RUFFIN ROAD • SAN DIEGO CA 92123

TITLE: ASSEMBLY — S. S. INTR. SAFE FEM

SIZE	DRAWING NO.	CHANGE LETTER
D	231-4570-01	D

SCALE NONE | DO NOT SCALE DRAWING | SHEET 1 OF 6



UNLESS OTHERWISE NOTED:

1. ALL RESISTORS ARE IN OHMS, Ω ± 5% 1/4 W CC.
2. ALL CAPACITORS ARE IN µF.
3. ALL DIODES ARE IN914.
4. □ INDICATES PI PIN NUMBERS.

(5) THIS RESISTOR MUST BE FLAMEPROOF.

SCHEMATIC-
SOLID STATE INTR. SAFE FEM
231-6570-00C

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM	ML	231-4570-01	D
	MODEL NO. 235	DATE 11-10-81	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB SOLID STATE FEM	230-2400-03	1	
2	SCHEMATIC	231-6570-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COM(8 DIP) (NL)	965-580-00	1	Z24
7	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z15
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z8
9	IC, 4066 QUAD MUX CMOS (RCA)	965-587-06	1	Z13
10	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z10
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z6
12	IC, 4040 12BIT BIN CTR (MO,FC)	965-587-46	1	Z9
13	IC, 4555 DUAL 10F4 NI(MO,FC,NL)	965-587-68	1	Z14
14				
15				
16	IC, 4572 INV, NOR, NAND CMOS (MO)	965-618-00	2	Z16,25
17	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z23
18				
19	IC, TL060CP OPAMP (TI)	965-646-00	1	Z19
20	IC, TL061CP OPAMP (TI)	965-646-01	2	Z20,21
21	IC, TL317LP VREG (TI)	965-645-00	1	Z22
22	RES, FILM RN60C, 2.49K	920-424-91	1	R60
23	RES, FILM RN55E, 500	922-450-00	1	R61
23	RES, FILM RN60C, 1% 499K	920-449-93	1	R79

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MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM	ML	231-4570-01	D
	MODEL NO. 235	DATE 11-10-81	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C 46.4K	920-446-42	1	R56
26	RES, FILM RN55D 1% 10K	924-310-02	2	R53,54
27	RES, FLAMEPROOF, 1/4W 100	940-010-00	2	R58, 59
28	RES, FILM RN55C 1% 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	2	R91
30				
31	RES, CARBON 1/4W ±5%, 1K	942-201-02	2	R41,42
32				
33	RES, CARBON 1/4W ±5%, 100K	942-201-04	7	R62,73,84,87, 66,74,90
34	RES, CARBON 1/4W ±5%, 150	942-201-51	2	R52,82
35	RES, CARBON 1/4W ±5%, 150K	942-201-54	2	R88,71
36				
37	RES, CARBON 1/4W ±5%, 20K	942-202-03	7	R45-46,49-51,57 67
38	RES, CARBON 1/4W ±5%, 220	942-202-21	2	R69,80
39	RES, CARBON 1/4W ±5%, 220K	942-202-24	2	R81,83
40				
41	RES, CARBON 1/4W ±5%, 3.9K	942-203-92	1	R48
42	RES, CARBON 1/4W ±5%, 39K	942-203-93	2	R47,72
43	RES, CARBON 1/4W ±5%, 470	942-204-71	1	R70
44	RES, CARBON 1/4W ±5%, 4.7K	942-204-72	1	R94
45	RES, CARBON 1/4W ±5%, 47K	942-204-73	3	R85,86,68
46	RES, CARBON 1/4W ±5%, 680K	942-206-84	1	R89
47	RES, CARBON 1/2W ±5%, 2.2K	942-302-22	40	R1-40
48				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM	MODEL NO. 235	231-4570-01	D
		DATE 11-10-81	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52				
53	CAP, DISC, .01/500V (5GA)	900-021-04	45	C1-40,61,65,67, 73,84
54	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	4	C76,78,74,75
55	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	5	C62,63,77,83,85
56	CAP, PLP,/.1/200V, IMB(GA2C104K)	917-001-20	1	C79
57	CAP, PLP,.22/200V, IMB(GA2C224K)	917-022-20	1	C82
58	CAP, PLP,.47/200V, IMB(GA2C474K)	917-047-20	2	C66,68
59	CAP, .1 @ 50V VARADYNE	900-021-08	1	C81
60	CAP, SF, .0022/250V, SMS (32570)	918-002-25	1	C64
61	CAP, SF, .22/100V, SMS(B32570)	918-022-10	24	72 C41-60,80,70,71,
62				
63	CAP, SF, 1/100V SMS (B32571)	918-010-10	1	C69
64				
65				
66				
67	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	9	CR4-12
68				
69	DIODE, 1N5236B (7.5V)	961-523-62	1	CR2
70				
71	DIODE, 1N5240, 10V	961-524-00	1	CR1
72				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM	MODEL NO. 235	231-4570-01	D
		DATE 11-10-81	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76	GRADED 4016	000-7700-00	4	Z11,12,17,18
77	SELECTED 4051 CMOS MULTI	000-8050-00	1	Z7
78	SELECTED 4052 CMOS MULTI	000-8051-00	5	Z1-5
79	FET, 2202 (NJ,LO-LK,GP)	100-722-02	3	Q2,14,15
80	TRANSISTOR, (SELECTED-COLOR DOT)	220-7200-01	1	Q1
81	TRANSFORMER, INTERFACE	967-0001-01	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
84	POT, 500 CERMET (72XL)	960-015-07	1	R55
85	POT, 25K MT2X253	960-015-15	1	R43
86	XSTR, PN2222 (NPNA92)	962-222-20	3	Q8,9,11
87	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	4	Q3,4,10,13
88	FET, NPD5566(NJ,LO,NSE,8BIT)NL	962-556-60	1	Q5
89	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,12
90	OPTO, FCD831B (FC)	965-570-03	2	OC1,OC2
91	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
92	SPACER, 1/8 X 6A2 (L6310-2-2A)	991-020-88	2	
93	IC SOCKET, 16DIP PC (316AG5DR)	992-010-22	6	
94	DISS-O-PAD, .250 OD. X .125 ID X .03 BIVAR INC. TO-16-03	979-020-11	6	
95				
96				

ZONE	LTR	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X1	R & D RELEASE	RP	4-4-83	J Carter
		B	PROD REL PER E.O. 2-11210	D.C.	5/4/83	
		C	REVISED PER E.O. 2-11220	DC	5/20/83	

6 R1 THRU R40 ARE 2.2K, 1/2 W C.C.

7 RUBBER STAMP ASSY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS ON FAR (CIRCUIT) SIDE.

8 INSTALL 3 DISS-O-PADS (TO 16-03) UNDER TERM STRIP. ONE IN CENTER AND ONE ON EACH END.

9 R58 AND R59 MUST BE FLAMEPROOF.

10 INSTALL SOLID 24 AWG. TEFLON INSULATED BUS WIRE.

NOTES: UNLESS OTHERWISE SPECIFIED

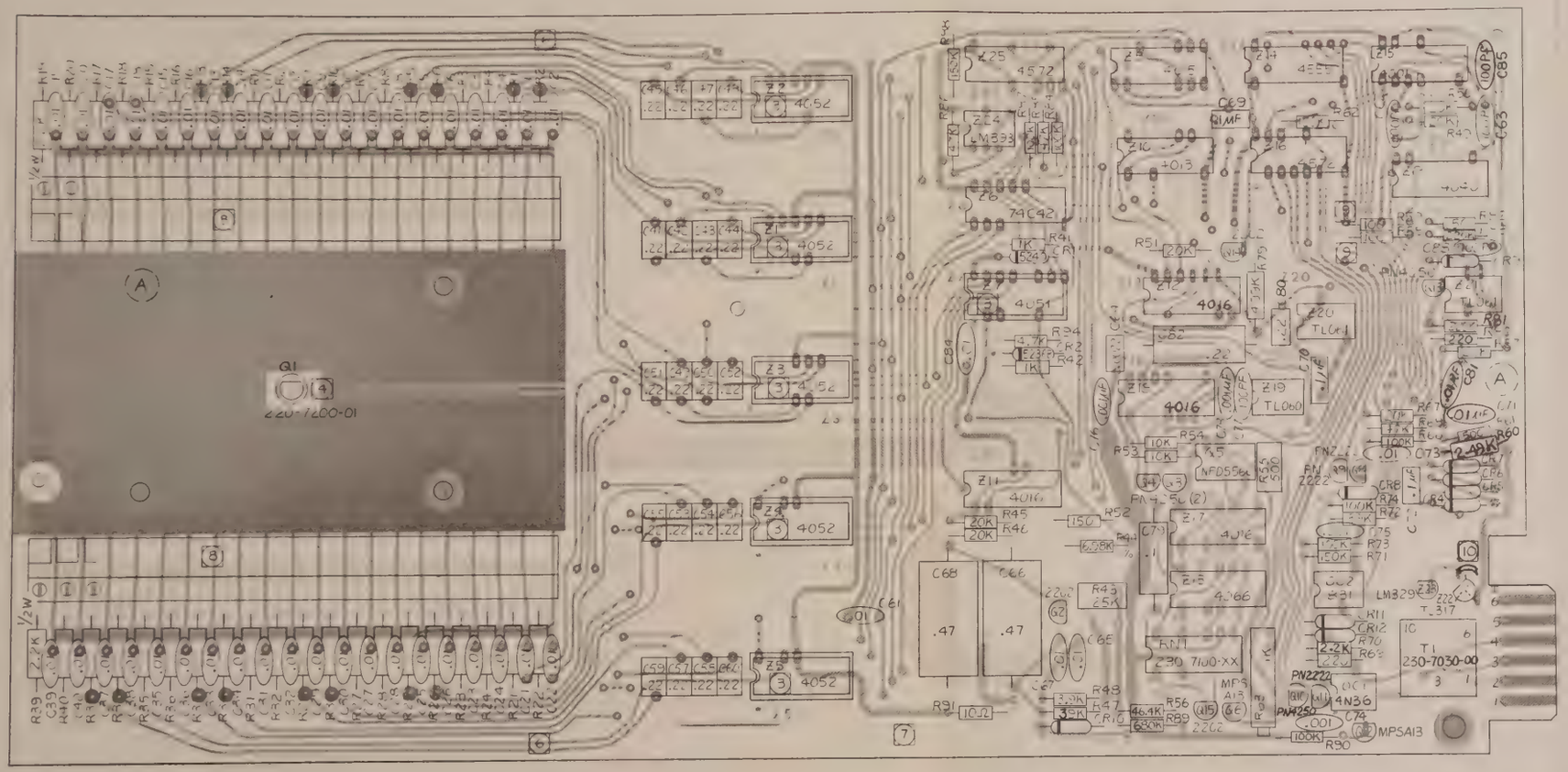
1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.
2. INSTALL HARDWARE PER CHART.

HARDWARE INSTALLATION CHART			
SYM	QTY	PART NUMBER	REMARKS
A	2	991-020-88	SPACER, FARSIDE

3 INSTALL 16 PIN SOCKET.

4 COMP HEIGHT NOT TO EXCEED 5/16 INCH FROM BOARD.

5. ALL DIODES ARE 1N914.



CONTROLLED DOCUMENT

PRIOR NOTIFICATION MUST BE MADE TO L'INSTITUT NATIONAL DES INDUSTRIES EXTRACTIVES (INIEX) BEFORE ANY CHANGES ARE MADE TO THIS DOCUMENT.

ASSEMBLY NO	SUPERSEDES	
	DES/ENG	R Price 4/4/83
	DRAWN	H. LAM 4-4-83
	CHECK	R Price 4/4/83
	APPR.	J Carter 4/4/83

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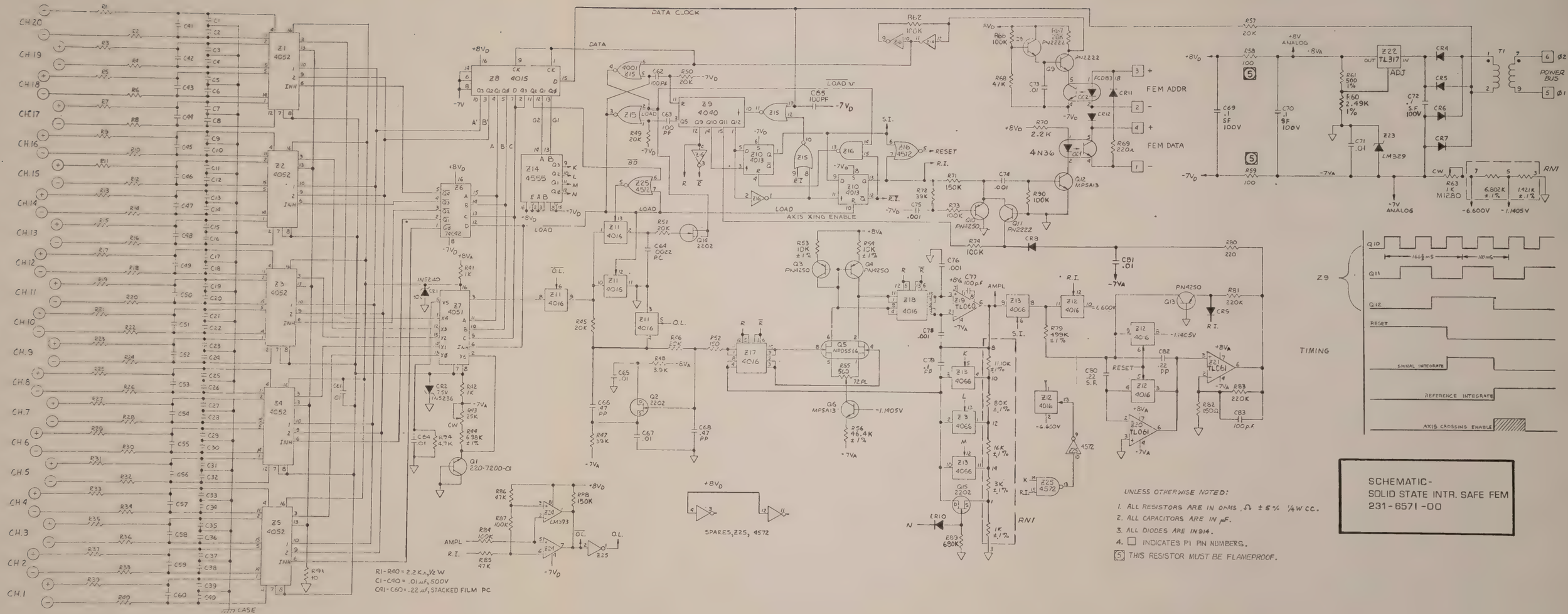
DORIC DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

TITLE	ASSY, S.S. INTR. SAFE FEM (CEN)	SIZE D	DRAWING NO. 231-4571-00 C
		SCALE NONE	DO NOT SCALE DRAWING SHEET 1 OF 6



UNLESS OTHERWISE NOTED:

1. ALL RESISTORS ARE IN OHMS, Ω ± 5% ¼W CC.
2. ALL CAPACITORS ARE IN µF.
3. ALL DIODES ARE IN914.
4. □ INDICATES P1 PIN NUMBERS.

5 THIS RESISTOR MUST BE FLAMEPROOF.

SCHEMATIC-
SOLID STATE INTR. SAFE FEM
231-6571-00

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB, ASSEMBLY SOLID STATE INTR. SAFE FEM (CEN)	MODEL NO. 235	231-4571-00 DATE 3-31-83	C SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB SOLID STATE FEM	230-2400-03	1	
2	SCHEM SOLID STATE FEM	231-6571-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COM(8DIP)(NL)	965-580-00	1	Z24
7	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z15
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z8
9	IC, 4066 QUAD MUX CMOS (RCA)	965-587-06	1	Z13
10	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z10
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z6
12	IC, 4040 12 BIT BIN CTR (MO,FC)	965-587-46	1	Z9
13	IC, 4555 DUAL 10F4 NI(MO,FC,NL)	965-587-68	1	Z14
14				
15				
16	IC, 4572 INV, NOR, NAND CMOS(MO)	965-618-00	2	Z16,Z25
17	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z23
18				
19	IC, TL060CP OPAMP (TI)	965-646-00	1	Z19
20	IC, TL061CP OPAMP (TI)	965-646-01	2	Z20,Z21
21	IC, TL317LP VREG (TI)	965-645-00	1	Z22
22	RES, FILM RN60C, 2.49K	920-424-91	1	R60
23	RES, FILM RN55E, 500	922-450-00	1	R61
24	RES, FILM RN60C, 1% 499K	920-449-93	1	R79

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM (CEN)	MODEL NO. 235	231-4571-00	C
		DATE 3-31-83	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C 46.4K	920-446-42	1	R56
26	RES, FILM RN55D 1%, 10K	924-310-02	2	R53,R54
27	RES, FLAMEPROOF, 1/4W, 100	940-010-00	2	R58,R59
28	RES, FILM RN55C 1%, 6.98K	924-469-81	1	R44
29	RES, CARBON 1/4W ±5%, 10	942-201-00	1	R91
30				
31	RES, CARBON 1/4W ±5%, 1K	942-201-02	2	R41,R42
32				
33	RES, CARBON 1/4W ±5%, 100K	942-201-04	7	R62,R66,R73,R74 R84,R87,R90
34	RES, CARBON 1/4W ±5%, 150	942-201-51	2	R52,R82
35	RES, CARBON 1/4W ±5%, 150K	942-201-54	2	R71,R88
36				
37	RES, CARBON 1/4W ±5%, 20K	942-202-03	7	R45,R46,R49-51, R57,R67
38	RES, CARBON 1/4W ±5%, 220	942-202-21	2	R69,R80
39	RES, CARBON 1/4W ±5%, 220K	942-202-24	2	R81,R83
40	RES, CARBON 1/4W ±5%, 2.2K	942-202-22	1	R70
41	RES, CARBON 1/4W ±5%, 3.9K	942-203-92	1	R48
42	RES, CARBON 1/4W ±5%, 39K	942-203-93	2	R47,R72
43				
44	RES, CARBON 1/4W ±5%, 4.7K	942-204-72	1	R94
45	RES, CARBON 1/4W ±5%, 47K	942-204-73	3	R68,R85,R86
46	RES, CARBON 1/4W ±5%, 680K	942-206-84	1	R89
47	RES, CARBON 1/2W ±5%, 2.2K	942-302-22	40	R1-40
48				

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MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM (CEN)	ML	231-4571-00	C
	MODEL NO. 235	DATE 3-31-83	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52				
53	CAP, DISC, .01/500V (5GA)	900-021-04	47	C1-40,C61,C65,C67, C71,C73,C81,C84
54	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	4	C74-76,C78
55	CAP, DISC, 100 pf @ 1KV (5GA)	901-011-01	5	C62,C63,C77,C83 C85
56	CAP, PLP .1/20V, IMB(GA2C104K)	917-001-20	1	C79
57	CAP, PLP .22/220V, IMB(GA2C224K)	917-022-20	1	C82
58	CAP, PLP .47/200V, IMB(GA2C474K)	917-047-20	2	C66,C68
59				
60	CAP, SF, .0022/250V, SMS (32570)	918-002-25	1	C64
61	CAP, SF, .22/100V, SMS (B32570)	918-022-10	21	C41-60,C80
62				
63	CAP, SF, .1/100V SMS (B32570)	918-001-10	3	C69,C70,C72
64				
65				
66				
67	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	9	CR4-12
68				
69	DIODE, 1N5236B (7.5V)	961-523-62	1	CR2
70				
71	DIODE, 1N5240, 10V	961-524-00	1	CR1
72				

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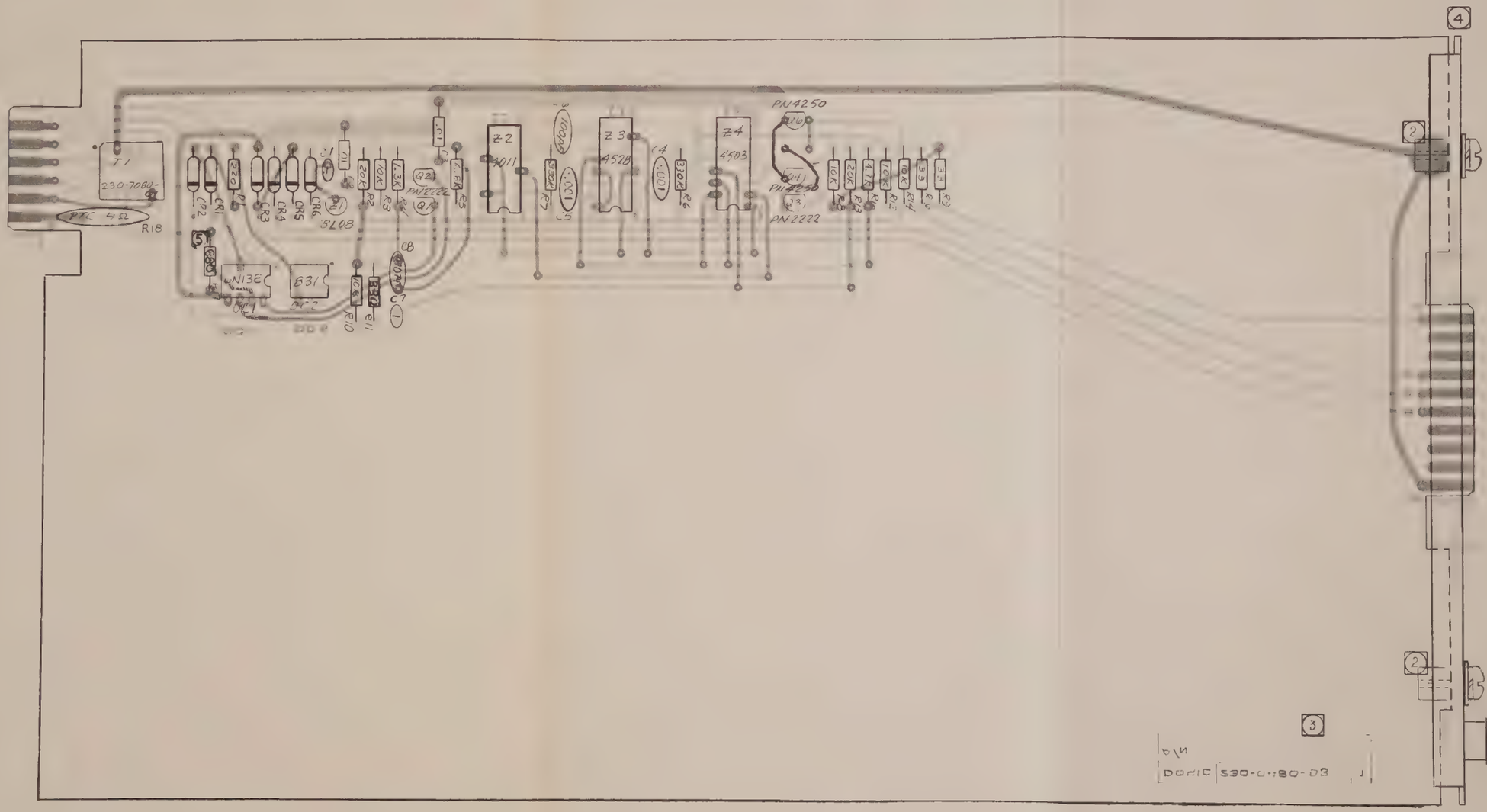
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE INTR. SAFE FEM (CEN)	MODEL NO. 235	231-4571-00	C
		DATE 3-31-83	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76	GRADED 4016	000-7700-00	4	Z11,Z12,Z17,Z18
77	SELECTED 4051 CMOS MULTI	000-8050-00	1	Z7
78	SELECTED 4052 CMOS MULTI	000-8051-00	5	Z1-5
79	FET, 2202 (NJ,LO-LK, GP)	100-722-02	3	Q2,Q14,Q15
80	TRANSISTOR, (SELECTED-COLOR DOT)	220-7200-01	1	Q1
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
84	POT, 500 CERMET (72XL)	960-015-07	1	R55
85	POT, 25K MT2X253	960-015-15	1	R43
86	XSTR, PN2222 (NPNA92)	962-222-20	3	Q8,Q9,Q11
87	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	4	Q3,Q4,Q10,Q13
88	FET, NPD5566(NJ,LO,NSE,8BIT) NL	962-556-60	1	Q5
89	XSTR, MPSA13 (NPNA/DRL92) (M)	964-040-03	2	Q6,Q12
90	OPTO, FCD831B (FC)	965-570-03	1	OC2
91	T.S. 20P ELCTVT 8145 251352053	973-010-55	2	
92	SPACER, 1/8 X 6A2 (L6310-2-2A)	991-020-88	2	
93	IC SOCKET, 16 DIP PC (316AG5DR)	992-010-22	6	
94	DISS-O-PAD, .250 OD X .125 ID X .03 BIVAR INC. TO-16-03	979-020-11	6	
95	OPTO, 4N36 (GE)(MOT)	965-5700-11	1	OC1
96				


T1
230-7080-
PTC 4Ω
R18
CR2
CR1
R1
CR3
CR4
CR5
CR6
8678
R2
R3
R4
R5
Q2
PN2222
Z2
4011
Z3
4528
Z4
4503
C4
.01
R6
PN4250
Q6
Q4
Q3
PN2222
R7
C5
R8
R9
R10
R11
R12
R13
R14
R15
C6
C7
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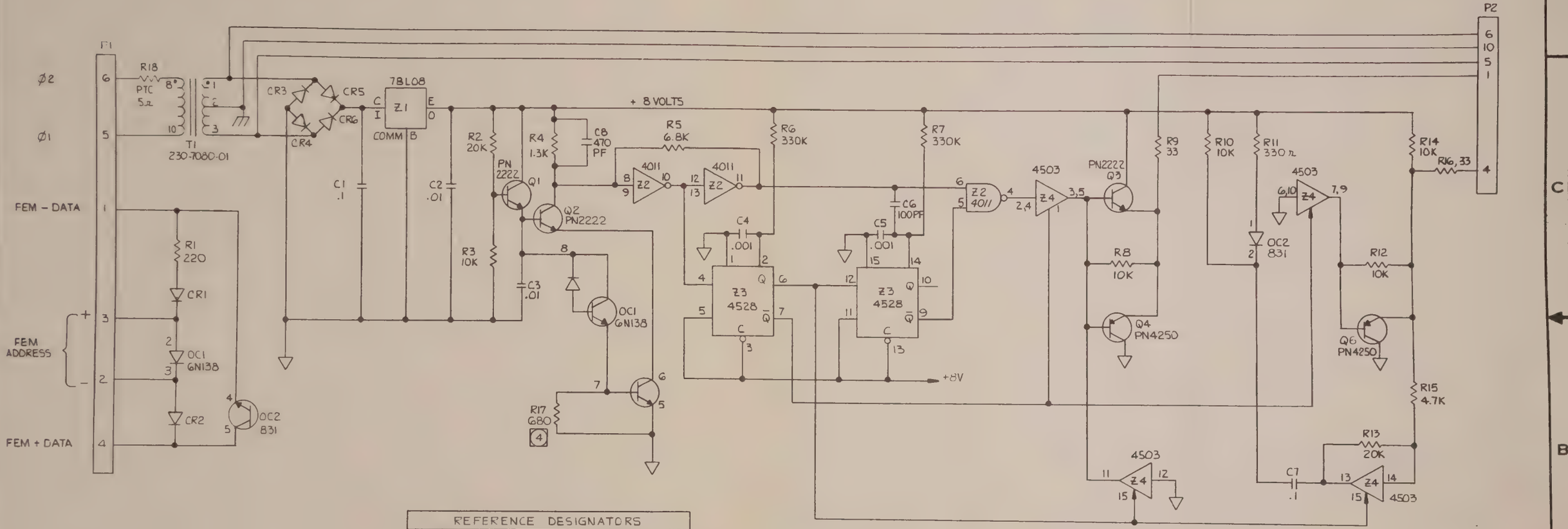
C41
C42
C43
C44
C45

NOTES: UNLESS OTHERWISE SPECIFIED

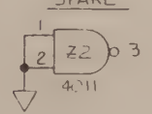
1. DIODES ARE 1N914
2. NPN'S ARE PN2222 PNPS ARE PN4250
3. CAPACITANCE IN uF RESISTANCE IN OHMS 1/4 WATT, +/- 5%
4. RESISTOR (R17) S.O.T VALUE COULD CHANGE AT TEST.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		D	REDRAWN REVISED PER E.O. 2-10289 & 2-10321	DC	3-23-81	
		E	REVISED PER E.O. 2-10972		3-27-81	



REFERENCE DESIGNATORS		
LAST USED		UNUSED
RESISTORS	R18	Q5
CAPACITORS	C8	
DIODES	CR7	
CONNECTORS	P1, P2	
TRANSFORMER	T1	
TRANSISTOR	Q7	
IC'S	Z4	
OSCILLATOR	OC2	

SPARE



ASSEMBLY NO. 230-4480-03E	SUPERSEDES 230-6480-03		
	DES/ENG	D. KNOX	3/21/79
	DRAWN	Gloria Ruiz	3/11/81
	CHECK	J. Galtin	3/23/81
	APPR.		

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TITLE: SCHEMATIC, REMOTE FEM INTERFACE

SIZE: D | DRAWING NO. 230-6480-03 | CHANGE LETTER E

SCALE — | DO NOT SCALE DRAWING | SHEET 1 OF 1

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY PCB, REMOTE FEM INTERFACE	MODEL NO. 230A 235	DATE 6-25-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, REMOTE FEM INTERFACE	230-2480-03	1	
2	SCHEMATIC	230-6480-03	1	
3	TEST SPEC		1	
4				
5				
6	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z2
7	IC, 4528 MONO-VIB CMOS (FC,MO)	965-587-14	1	Z3
8	IC, 4503 TRI-STATE HEX BUFFER	965-587-69	1	Z4
9	IC, LM78L08 ACZ	965-637-01	1	Z1
10				
11				
12				
13				
14				
15	RES, 1/4W ±5%, 330	942-203-31	1	R11
16	RES, 1/4W ±5%, 10K	942-201-03	5	R3,R8,R10,R12, R14
17	RES, 1/4W ±5%, 20K	942-202-03	2	R2,R13
18	RES, 1/4W ±5%, 220	942-202-21	1	R1
19	RES, 1/4W ±5%, 33	942-203-30	2	R9,R16
20	RES, 1/4W ±5%, 330K	942-203-34	2	R6,R1
21	RES, 1/4W ±5%, 4.7K	942-204-72	1	R15
22	RES, 1/4W ±5%, 6.8K	942-206-82	1	R5
23	RES, 1/4W ±5%, 1.3K	941-201-32	1	R4
24	RES, 1/4W ±5%, 680	942-206-81	1	R17

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY PCB, REMOTE FEM INTERFACE	MODEL NO. 230A 235	230-4480-03	G
		DATE 6-25-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26				
27				
28				
29				
30	CAP, .1MF@50V(3429-050E-104Z)	900-021-02	2	C1,C7
31	CAP, AXIAL .01/50V 180/25V050A	900-021-07	2	C2,C3
32	CAP, DISC. .001@ 1KV (5GA)	900-081-03	2	C4,C5
33	CAP, DISC. 100 PF @ 1KV (5GA)	901-011-01	1	C6
34	CAP, DISC. 470 PF @ 1KV (5GA)	901-014-71	1	C8
35				
36				
37				
38				
39	DIODE, 1N914 (1N4148) (TD,FC,T1)	961-091-40	6	CR1-CR6
40				
41				
42				
43				
44				
45	XFMR, REMOTE FEM INTER	230-7080-01	1	T1
46	THERMISTOR, RL5506-5-110-50-PTX-5015-PTF	955-000-05	1	R18
47	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q1,Q2,Q3
48	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	2	Q4,Q6

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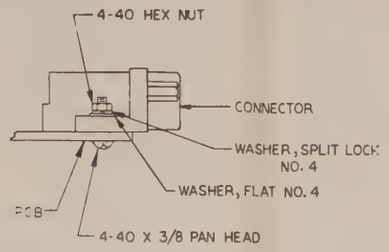
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY PCB, REMOTE FEM INTERFACE	MODEL NO. 230A 235	DATE 6-25-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	OPTO, FCD831B (FC)	965-570-03	1	OC2
50	CHASSIS FSTNR, 632B2 (US1590B1)	991-020-26	2	
51	OPTO 6N138	965-570-01	1	OC1
	THE FOLLOWING PARTS ARE TO BE ADDED IN TEST:			
51	REAR PANEL REMOTE FEM INT	230-2890-00	1	
52	SCREW MAC. 6-32 X 3/8: PHMS	980-632-038	2	
53	WASHER FLAT #6	986-100-06	3	
54	WASHER SPLITLOCK #6	986-200-06	3	
55	SCREW, PAN HEAD, PHILLIPS, 6-32 X 1/2 LG	980-632-050	1	



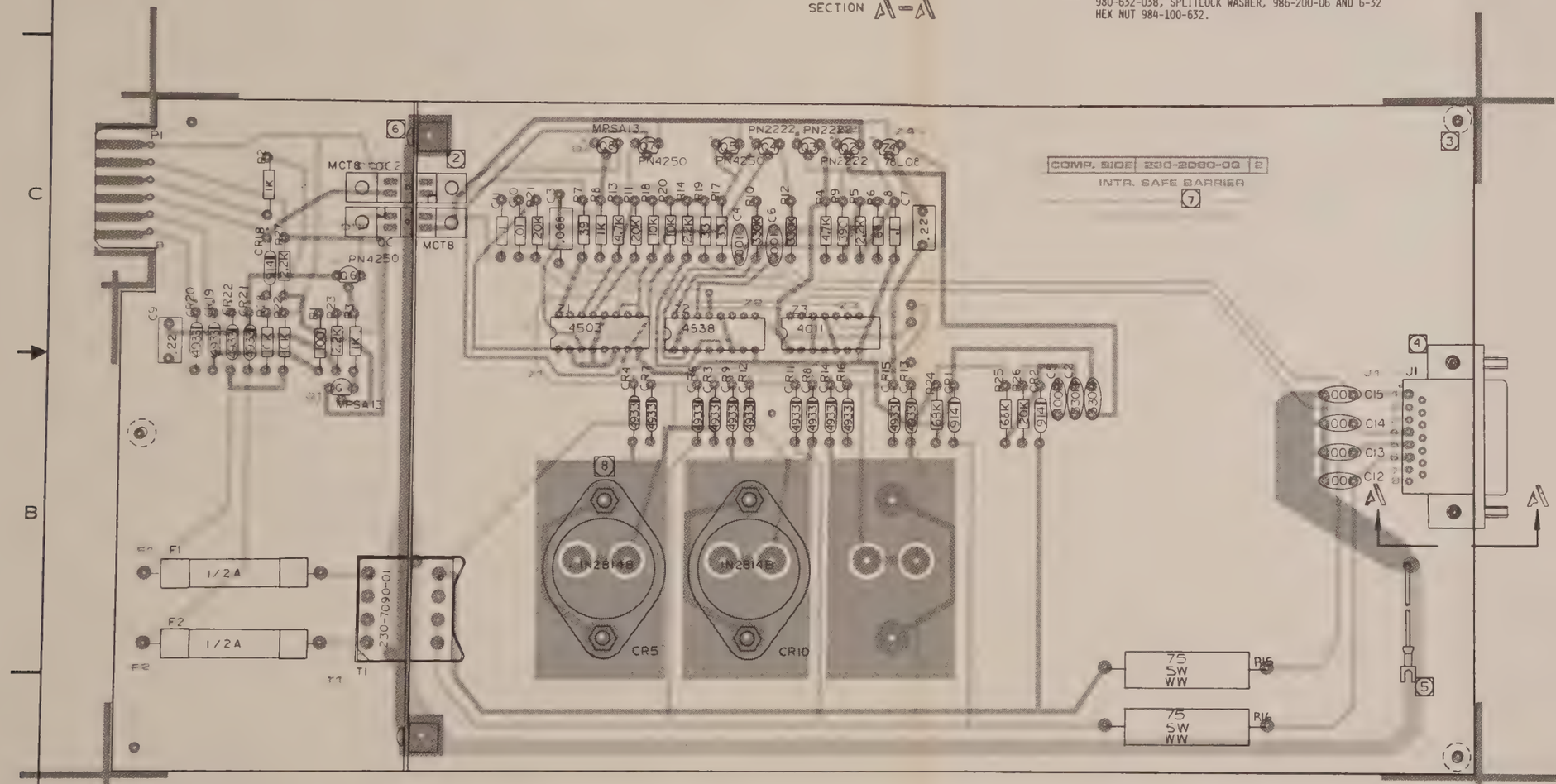
SECTION A-A

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.
2. INSTALL CHASSIS FASTENER 991-020-26, (2) PLCS.
3. INSTALL SPACER 991-020-88, (3) PLCS, FAR SIDE.
4. INSTALL SCREW 4-40 X 3/8 PHMS 980-440-038, FLAT WASHER 986-100-04, SPLITLOCK WASHER 986-200-04, AND RADIAL NUT 984-200-440, TYP. (2) PLCS (SEE SECTION A-A).
5. INSTALL TERMINATED GROUND WIRE 993-300-03.
6. INSTALL BARRIER 230-3020-XX USING (2) EACH 6-32 X 3/8 PHMS 980-632-038, FLAT WASHER 986-100-06, AND SPLITLOCK WASHER 986-200-06.
7. RUBBER STAMP ASSY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS (FAR SIDE).
8. INSTALL CR5 AND CR10 USING (2) EACH 6-32 X 3/8 PHMS, 980-632-038, SPLITLOCK WASHER, 986-200-06 AND 6-32 HEX NUT 984-100-632.

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A1	LIMITED USAGE RELEASE	—	—	—
		A2	REVISED AND REDRAWN PER E.O. 2-10207	G.R.	5/14/81	J. Crabtree
		B	PROD RELEASE PER E.O. 2-10730	A.D.	[illegible]	A. Damon
		C	REVISED PER E.O. 2-10918	A.D.	2-3-82	M. Cook
		D	REVISED PER E.O. 2-10938	mc	5/7/82	JC/DWS
		B	REVISED PER E.O. 2-11003	RP	5-13-82	DWS
		C	REVISED PER E.O. 2-11064	RP	3-28-83	J. Crabtree



CONTROLLED DOCUMENT

PRIOR NOTIFICATION MUST BE MADE TO FACTORY MUTUAL SYSTEMS BEFORE ANY CHANGES ARE MADE TO THIS DOCUMENT.

HOLE TOLERANCES

.000-.250 DIA	+.004-.002
.251-.500 DIA	+.006-.002
.501-1.00 DIA	+.010-.005

SUPERSEDES 230-4080-00 D

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NOTES UNLESS SPECIFIED

1. TOLERANCES .XX ±.03 DIMENSIONED ANGLES .XXX ±.010 ±½°
2. BREAK ALL SHARP EDGES .010 APPROX
3. MACH SURFACES
4. ALL DIM IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

USED ON 235

NEXT ASSY. 231-5020-XX

DRAWN	R. Mefford	10/30/80
CHECK	J. Crabtree	3/23/81
APPR.	A. Pride	5-25-81

MATERIAL

FINISH

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO CA 92123

TITLE ASSEMBLY, PCB, INTR. SAFETY BARRIER

SIZE	CODE IDENT. NO	DRAWING NO	CHANGE LETTER
D		230-4080-01	C

SCALE 1:1 DO NOT SCALE DRAWING SHEET 1 OF 5

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4 WATT ±5%, AND RESISTANCE IS IN OHMS.
2. ALL DIODES ARE 1N4933.
3. ALL CAPACITANCE IS IN MICRO FARADS (MF).
4. OPTION FOR 16 BIT CONFIGURATION. (BREAK CONNECTION AND ADD JUMPER)

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A2	REVISED AND REDRAWN PER E.O. 2-10207.	DWS	3/15/80	
		B	PROD RELEASE PER E.O. 2-10730	A.D.	10-20-80	
		C	REVISED PER E.O. 2-10918	A.D.	6-3-81	
		B	REVISED PER E.O. 2-11003	DS	5/7/82	DWS
		C	REVISED PER E.O. 2-11064	DS	7-21-82	

P1
T1 230-7090-01
F2 1/2A
F1 1/2A
Ø1
Ø2
R26 10K
CR19
CR21
C9 .22/100V
R22 10K
CR20
CR22
90T
CR1/1N914
C1 330PF
R24 68K
R25 68K
C2 330PF
CR2 1N914
CR3
CR4
CR5 IN2814B 16V
CR6
CR7
CR8
CR9
CR10 IN2814B 16V
CR11
CR12
CR13
CR14
CR15
CR16
78L06 C Z4 E
IN
OUT
COMM
B
C7 .22 100V
C8 .1
R16 75 5W/WW
R15 75 5W/WW
J1
C12 .001
C13 .001
C14 .001
C15 .001
R1 100
R23 2.2K
Q6 PN4250
R3 1K
C5 100PF
R26 20K
R4 4.7K
+8V
R10 330K
R12 330K
C11 .1
OC1 MCT-8
R9 390
Q2 PN2222
Q3 PN2222
R6 68
R5 2.2K
R7 39
Z3 4011
C4 .001
C6 .001
Z2 4538
CD
4503
Z1
Q4 PN2222
R17 33
R18 10K
Q5 PN4250
R21 20K
C10 .01
R14 2.2K
R13 4.7K
R11 20K
R19 33
R20 10K
Q7 PN4250
FEM ADDRESS + 3
FEM ADDRESS − 2
FEM DATA + 4
FEM DATA − 1
R2 1K
R27 2.2K
Q1 MPSA13
CR18 1N914
OC2 MCT-8
Q8 MPSA13
R8 1K
C3 .068 100V
METAL BARRIER 230-3020-XX

CONTROLLED DOCUMENT
PRIOR NOTIFICATION MUST BE MADE TO FACTORY MUTUAL SYSTEMS BEFORE ANY CHANGES ARE MADE TO THIS DOCUMENT.

REFERENCE DESIGNATORS	
LAST USED	UNUSED
RESISTORS R28	
CAPACITORS C15	
DIODES CR19	CR17
TRANSISTOR	
TRANSFORMER T1	
CONNECTOR P1	
SOLDER	

ASSEMBLY NO. 230-4080-01	SUPERSEDES 230-6080-00 B		
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC	DES/ENG D. KNOX	3/20/81	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO, CA 92123
	DRAWN P.K. Mafford	10/23/80	TITLE SCHEMATIC - INTRINSIC SAFETY BARRIER CARD
	CHECK D SEXTON		SIZE D DRAWING NO. 230-6080-01 CHANGE LETTER C
	APPR.	8-25-82	SCALE NONE DO NOT SCALE DRAWING SHEET 1 OF 1

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSY, PCB INTRSC SAFE BARRIER	MODEL NO. 235	DATE 6-27-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB INTRINSICALLY SAFE	230-2080-03	1	
2	SCHEMATIC, INTRINSICALLY SAFE	230-6080-01	1	
3	TEST SPEC, INTRINSICALLY SAFE		1	
4				
5				
6	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z3
7	IC, 4538 MONO-VIB CMOS (FC,MO)	965-587-72	1	Z2
8	IC, 4503 TRI-STATE HEX BUFFER	965-587-69	1	Z1
9	IC, LM78L08 ACZ	965-637-01	1	Z4
10				
11				
12				
13				
14				
15				
16	RES, WW 5W 75 VC5E F.P. CLAROSTAT	936-575-06	2	R15, R16
17				
18	RES, 1/4W ±5%, 100	942-201-01	1	R1
19	RES, 1/4W ±5%, 1K	942-201-02	3	R2,R3,R8
20	RES, 1/4W ±5%, 10K	942-201-03	4	R18,R20,R22,R28
21	RES, 1/4W ±5%, 390	942-203-91	1	R9
22	RES, 1/4W ±5%, 39	942-203-90	1	R7
23	RES, 1/4W ±5%, 20K	942-202-03	3	R11,R21,R26
24	RES, 1/4W ±5%, 33	942-203-30	2	R17,R19

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY,PCB INTRSC SAFE BARRIER	MODEL NO. 235	230-4080-01	C
		DATE 6-27-80	SHEET 4 OF 5

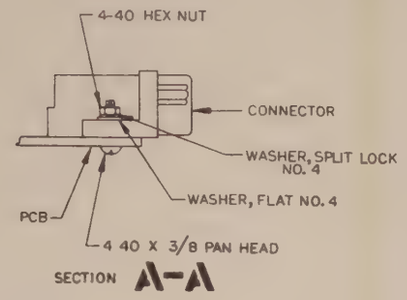
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, 1/4W ±5%, 330K	942-203-34	2	R10,R12
26	RES, 1/4W ±5%, 4.7K	942-204-72	2	R4,R13
27	RES, 1/4W ±5%, 68	942-206-80	1	R6
28	RES, 1/4W ±5%, 2.2K	942-202-22	4	R5,R14,R23,R27
29	RES, 1/4W ±5%, 68K	942-206-83	2	R24,R25
30				
31				
32				
33	CAP, AXIAL .1/50V VARADYNE 1802	900-021-08	2	C8,C11
34	CAP, AXIAL .01/50V 18012Z5U050A	900-021-07	1	C10
35	CAP, DISC .001 @ 1KV (5GA)	900-081-03	6	C4,C6, C12-C15
36	CAP, DISC 100PF @ 1KV (5GA)	901-011-01	1	C5
37	CAP, DISC 330PF @ 1KV (5GA)	901-013-31	2	C1,C2
38	CAP, POLYC .068 @ 100V BAZB	911-036-83	1	C3
39	CAP, .22 @ 100V (B32570)	918-022-10	2	C7,C9
40				
41				
42				
43	DIODE, 1N914 (1N4148) (TD,FC,TI	961-091-40	3	CR1,CR2,CR18
44	DIODE, 1N4933 (1A/50V,FAST) (MO)	961-493-30	16	CR3,CR4,CR6-CR9 CR11-CR16,CR19-22
45	DIODE, ZENER 1N2814B, 16V, MO.	961-535-54	2	CR5, CR10
46				
47				
48				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY, PCB INTRSC SAFE BARRIER	MODEL NO. 235	DATE 6-27-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52	BARRIER STRIP	230-3020-00	1	
53	TRANSFORMER ,INTRSC SAFE	230-7090- 01	1	T1
54	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q2-4
55	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	3	Q5,6,7
56				
57	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q1,Q8
58	FUSE, 1/2AMP PIGTL(318.500)	971-050-01	2	F1, F2
59				
60	CONN RECEPT 15PIN(AMP 745104-2)	973-010-76	1	J1
61	CHASSIS FSTNR, 632B2 (US1590B1)	991-020-26	2	
62	OPTICAL COUPLER (MCT-8)	965-570-07	2	OC1,OC2
63	SCREW, PAN HD. PHILLIPS 4-40 X 3/8	980-440-038	2	
64	SCREW, PAN HD. PHILLIPS 6-32 X 3/8	980-632-038	6	
65	WASHER, FLAT 6	986-100-06	2	
66	WASHER, SPLITLOCK 6	986-200-06	6	
67	NUT, HEX RADIAL 4-40	984-200-440	2	
68	SPACER, 1/8 X 6A2 (L6310-2-2A)	991-020-88	3	
69	ASSY,TERMINATED GROUND WIRE	993-300-03	1	
70	NUT, HEX 6-32	984-100-632	4	
71	WASHER, FLAT 4	986-100-04	2	
72	WASHER SPLITLOCK 4	986-200-04	2	

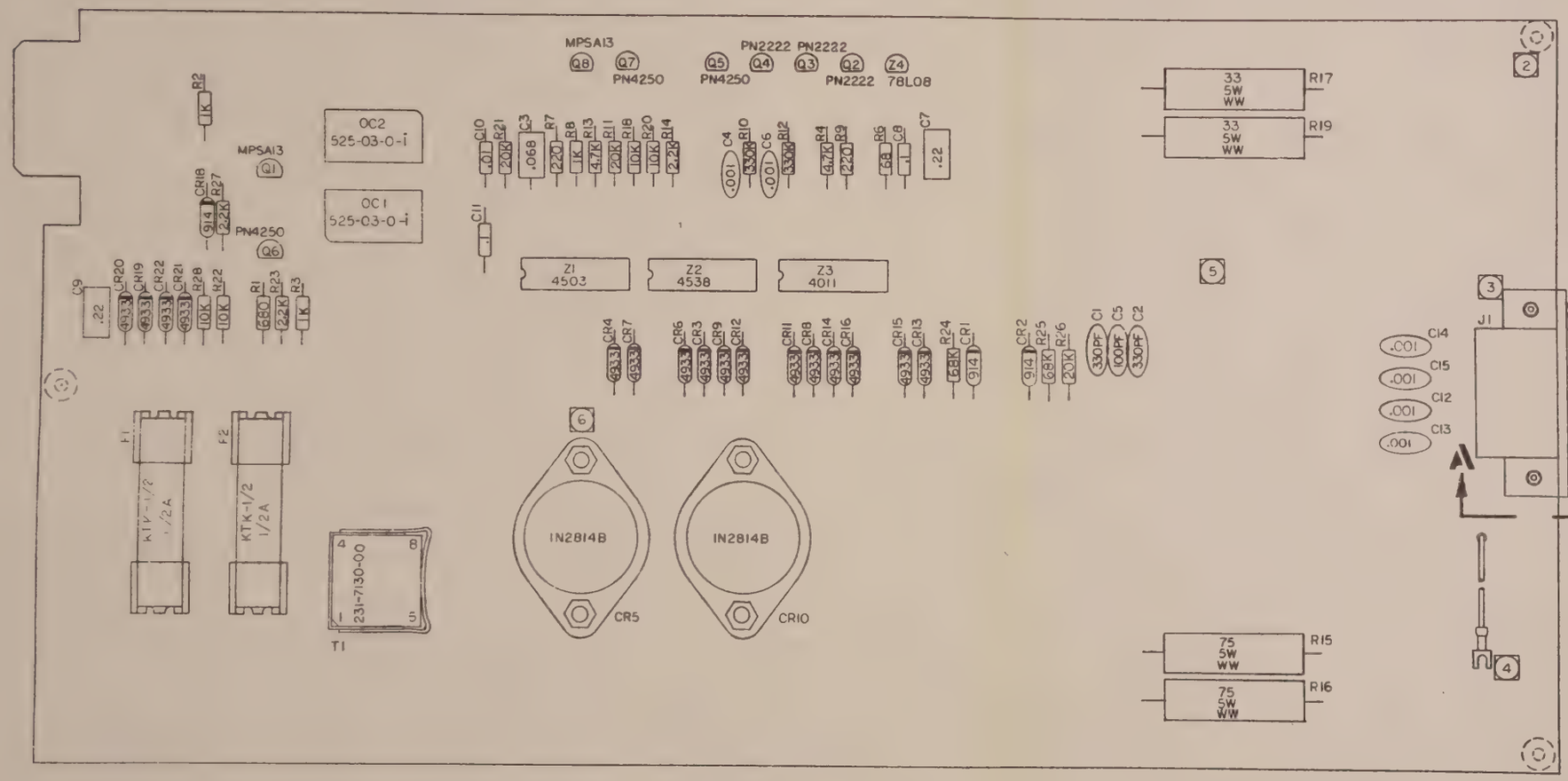


NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.
2. INSTALL SPACER 991-020-88, (3) PLCS, FAR SIDE.
3. INSTALL SCREW 4-40 X 3/8 PHMS 980-440-038, FLAT WASHER 986-100-04, SPLITLOCK WASHER 986-200-04, AND RADIAL NUT 984-200-440, TYP. (2) PLCS (SEE SECTION A-A).
4. INSTALL TERMINATED GROUND WIRE 993-300-03.
5. RUBBER STAMP ASSY NO. AND REVISION LETTER WITH .12 HIGH BLACK PERMANENT INK CHARACTERS (FAR SIDE).
6. INSTALL CR5 AND CR10 USING (2) EACH 6-32 X 3/8 PHMS, 980-632-038, SPLITLOCK WASHER, 986-200-06 AND 6-32 HEX NUT 984-100-632.

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X1	R & D RELEASE	[illegible]	[illegible]	[illegible]
		X2	R & D RELEASE	[illegible]	[illegible]	[illegible]
		B	PROD REL PER E.O. 2-11210	[illegible]	5/9/83	



CONTROLLED DOCUMENT
PRIOR NOTIFICATION MUST BE MADE TO L'INSTITUT NATIONAL DES INDUSTRIES EXTRACTIVES (INIEX) BEFORE ANY CHANGES ARE MADE TO THIS DOCUMENT.

HOLE TOLERANCES	NOTES UNLESS SPECIFIED	DRAWN	J. Boyer	1/6/83
.000-.200 DIA + .004-.002	1 TOLERANCES .XX ± .03 DIMENSIONED ANGLES .XXX ± .010 ± ½°	CHECK	W. C. Walker	1/27/83
.201-.500 DIA + .005-.002	2 BREAK ALL SHARP EDGES .010 APPROX.	APPR	[illegible]	[illegible]
.501-1.00 DIA + .010-.005	3 MACH. SURFACES J	MATERIAL		
SUPERSEDES	4 ALL DIM. IN INCHES			
	5 ALL TRUE POSITION TOLERANCES APPLY AT MMC			
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	NEXT ASSY 231-5025-XX			

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3800 RUFFIN ROAD • SAN DIEGO CA 92123

TITLE ASSEMBLY, PCB, INTRINSIC SAFETY BARRIER CARD (CEN)

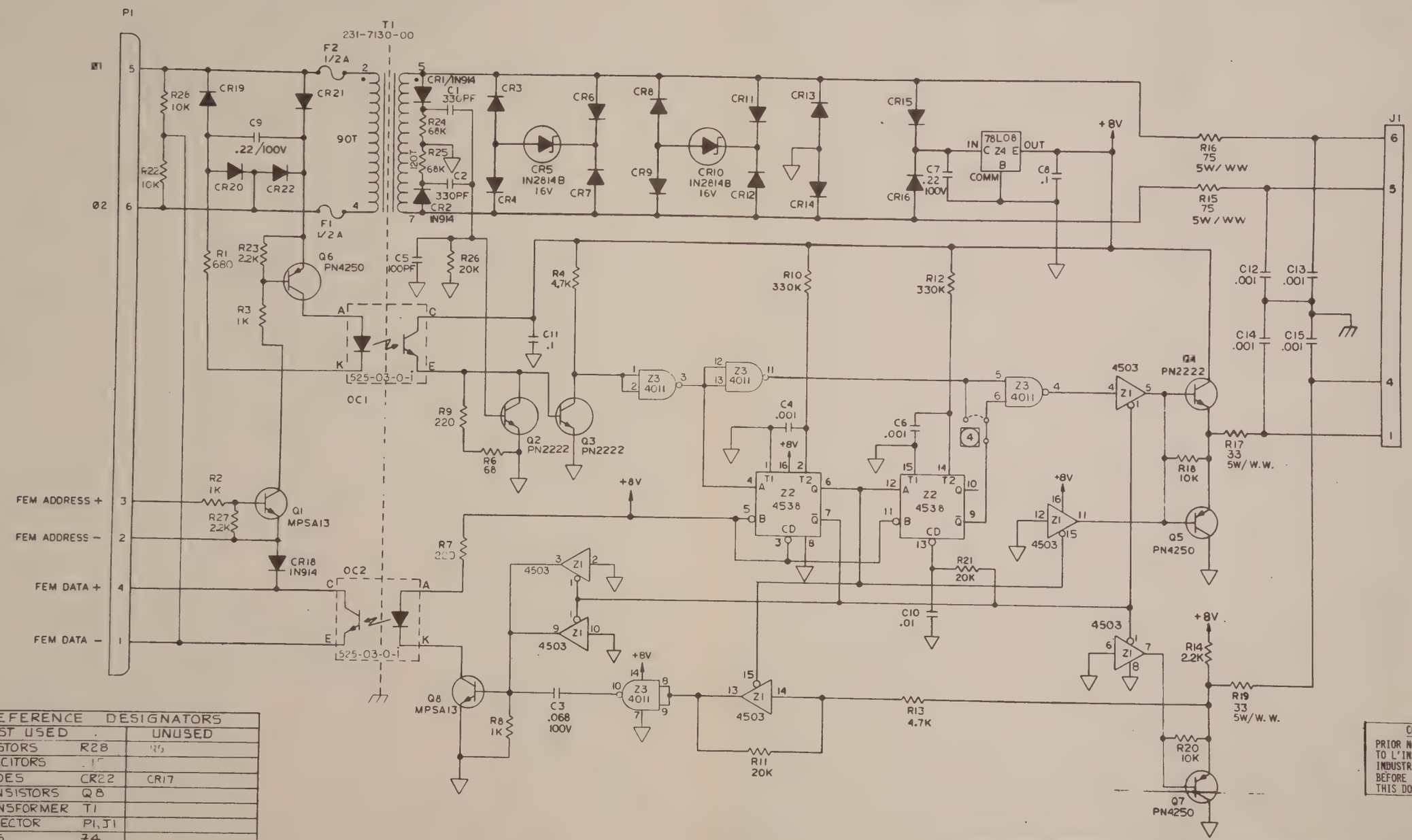
SIZE	CODE IDENT. NO	DRAWING NO	CHANGE LETTER
D		231-4620-00	B

SCALE 2:1 | DO NOT SCALE DRAWING | SHEET 1 OF 5

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4 WATT ±5%, AND RESISTANCE IS IN OHMS.
2. ALL DIODES ARE 1N4933.
3. ALL CAPACITANCE IS IN MICRO FARADS (MF).
4. OPTION FOR 16 BIT CONFIGURATION. (BREAK CONNECTION AND ADD JUMPER)

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X	R & D RELEASE	[illegible]	1-11-83	W C Wilson
		X1	R & D RELEASE	[illegible]	[illegible]	W C Wilson
		X2	R & D RELEASE	[illegible]	[illegible]	[illegible]
		B	PROD REL PER E.O. 2-11210	[illegible]	5/9/83	



REFERENCE DESIGNATORS		
LAST USED		UNUSED
RESISTORS	R28	R5
CAPACITORS	[illegible]	
DIODES	CR22	CR17
TRANSISTORS	Q8	
TRANSFORMER	T1	
CONNECTOR	P1, J1	
IC'S	Z4	
OPTO COUPLER	OC2	
FUSES	F2	

CONTROLLED DOCUMENT

PRIOR NOTIFICATION MUST BE MADE TO L'INSTITUT NATIONAL DES INDUSTRIES EXTRACTIVES (INIEX) BEFORE ANY CHANGES ARE MADE TO THIS DOCUMENT.

231-4620-XX

H. LAM 1-10-83

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3800 RUFFIN ROAD • SAN DIEGO, CA 92123

TITLE: SCHEMATIC - INTRINSIC SAFETY BARRIER CARD (CEN)

SIZE: D | DRAWING NO. 231-6620-00 | REV B

SCALE NONE | DO NOT SCALE DRAWING | SHEET 1 OF 1

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, INTRINICALLY SAFE BARRIER CARD (CEN)		231-4620-00	B
	MODEL NO. 235	DATE 1-27-83	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, INTR. SAFE BARRIER (CEN)	231-2620-00	1	
2	SCHEM, INTR. SAFE BARRIER (CEN)	231-6620-00	1	
3	TEST SPEC INTR. SAFE BARRIER (CEN)		1	
4				
5				
6	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z3
7	IC, 4538 MONO-VIB CMOS (FC,MO)	965-587-72	1	Z2
8	IC, 4503 TRI-STATE HEX BUFFER	965-587-69	1	Z1
9	IC, LM78L08 ACZ	965-637-01	1	Z4
10				
11				
12				
13				
14				
15				
16	RES, WW 5W 75 VC5E F.P. CLAROSTAT	936-575-06	2	R15,R16
17	RES, WW 5W, 33,VC5E F.P. CLAROSTAT	936-5750-07	2	R17,R19
18	RES, 1/4W ±5%, 220	942-202-21	2	R7,R9
19	RES, 1/4W ±5%, 1K	942-201-02	3	R2,R3,R8
20	RES, 1/4W ±5%, 10K	942-201-03	4	R18,R20,R22,R28
21	RES, 1/4W ±5%, 680	942-206-81	1	R1
22				
23	RES, 1/4W ±5%, 20K	942-202-03	3	R11,R21,R26
24				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV.
ASSEMBLY, PCB, INTRINICALLY SAFE BARRIER CARD (CEN)	ML	231-4620-00	B
	MODEL NO. 235	DATE 1-17-83	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, 1/4W ±5%, 330K	942-203-34	2	R10,R12
26	RES, 1/4W ±5%, 4.7K	942-204-72	2	R4,R13
27	RES, 1/4W ±5%, 68	942-206-80	1	R6
28	RES, 1/4W ±5%, 2.2K	942-202-22	3	R14,R23,R27
29	RES, 1/4W ±5%, 68K	942-206-83	2	R24,R25
30				
31				
32				
33	CAP, AXIAL .1/50V VARADYNE 1802	900-021-08	2	C8,C11
34	CAP, AXIAL .01/50V 1801Z5U050A	900-021-07	1	C10
35	CAP, DISC .001 @ 1KV (5GA)	900-081-03	6	C4,C6,C12-C15
36	CAP, DISC 100pf @ 1KV (5GA)	901-011-01	1	C5
37	CAP, DISC 330pf @ 1KV (5GA)	901-013-31	2	C1,C2
38	CAP, POLYC .068 @ 100V BAZB	911-036-83	1	C3
39	CAP, .22 @ 100V (B32570)	918-022-10	2	C7,C9
40				
41				
42				
43	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	3	CR1,CR3,CR18
44	DIODE, 1N4933 (1A/50V,FAST)(MO)	961-493-30	16	CR3,CR4,CR6-CR9 CR11-CR16,CR19-CR22
45	DIODE, ZENER 1N2814B, 16V, MO	961-535-54	2	CR5,CR10
46				
47				
48				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV
ASSEMBLY, PCB, INTRINICALLY SAFE BARRIER CARD (CEN)	ML	231-4620-00	B
	MODEL NO. 235	DATE 1-27-83	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52				
53	TRANSFORMER, INTR. SAFE (CEN)	231-7130-00	1	T1
54	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q2-Q4
55	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	3	Q5-Q7
56				
57	XSTR, MPSA13 (NPNA/DRL92) (M)	964-040-03	2	Q1,Q8
58	FUSE, 1/2A FB, BUSS KTK-1/2	971-0700-18	2	F1,F2
59	FUSECLIP, 13/32D BUSS 1A3400-09	971-0800-03	4	F1,F2
60	CONN RECEPT 15 PIN(AMP745104-2)	973-010-76	1	J1
61				
62	IC, OPTO ISO, ELFEIN 525-03-0-I	965-5700-10	2	OC1,OC2
63	SCREW, PAN HD. PHILLIPS 4-40 X 3/8	980-440-038	2	
64	SCREW, PAN HD. PHILLIPS 6-32 X 3/8	980-632-038	4	
65				
66	WASHER, SPLITLOCK NO. 6	986-200-06	4	
67	NUT, HEX RADIAL 4-40	984-200-440	2	
68	SPACER, 1/8 X 6A2 (L6310-2-2A)	991-020-88	3	
69	ASSY, TERMINATED GROUND WIRE	993-300-03	1	
70	NUT, HEX 6-32	984-100-632	4	
71	WASHER, FLAT NO. 4	986-100-04	2	
72	WASHER SPLITLOCK NO. 4	986-200-04	2	

ASSEMBLY-

PCB ALARM

231-4360-05B

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		D	ADDED BARS TO SIG. NAMES	T.L.	3/11/80	Crabtree
		B	REVISED PER E.O. 2-11058	MG	5/5/80	Crabtree
		C	REVISED PER E.O. 2-11402	MG	10/10/80	Crabtree

IC POWER DISTRIBUTION TABLE

REFERENCE DESIGNATORS	IC TYPE	POWER +5V	POWER GND	POWER VBB
1A	74LS245	20	10	—
2A, 3A, 4A, 5D	74LS04	14	7	—
5A	8797	16	8	—
2B, 2C, 2D, 2E	4334-3	—	9	18
3B	74LS27	14	7	—
4B	74LS30	14	7	—
5B 5K 5L	74LS14	14	7	—
3C	74LS138	16	8	—
3D, 4C, 5N	74LS02	14	7	—
5C	74LS175	16	8	—
4D 4E 4F	74LS10	14	7	—
3E 5M	74LS00	14	7	—
5E	74LS86	14	7	—
1H - 5H	74LS374	20	10	—
5J	74LS244	20	10	—
4M 4N	74C14	14	7	—

RAM MEMORY

SPARE

SPARE

CONTROL BUS
2A8
1A1

DATA BUS
2A8
1A1

ASSEMBLY NO. 231-4360-XX	SUPERSEDES		
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC	DES / ENG	David Page	5-2-80
	DRAWN		5-4-80
	CHECK		5-5-80
	APPR.		

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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TITLE: SCHEMATIC ALARM BOARD

SIZE D | DRAWING NO 231-6360-03 | CHANGE LETTER B

SCALE — DO NOT SCALE DRAWING | SHEET 1 OF 2

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

OUTPUT REGISTERS AND OPTO ISOLATORS

INPUT DATA SYSTEM AND CONTROL

REF DESIGNATORS	
LAST USED	DO NOT USE
RESISTOR R16	
CAPACITOR C26	
DIODE CR15	
R-NET RN8	
TRANSISTOR Q7	
SWITCH S3	S1
BATT. B1	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIODES ARE 1N914/1N4148
2. CAPACITANCE VALUES ARE IN uF
3. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
4. ALL OPTO ISOLATORS, 1KA, B THRU 4KA, B 1LA,B THRU 4LA, B, 1MA, B THRU 3MA, B ARE ILCT6.
5. ALL RAMS 2B 2C 2A AND 2E ARE 2114 TYPE CMOS RAMS.

SIZE	CODE IDENT. NO.	DRAWING NO	REVISION LETTER
D		231-6360-03	B
SCALE	DO NOT SCALE DRAWING	SHEET 2 OF 2	

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, ALARM BOARD	MODEL NO. 235	DATE 2-27-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, ALARM BOARD	231-2360-07	1	
2	SCHEMATIC	231-6360-03	1	
3	TEST SPEC			
4				
5				
6	IC, 74C14 HEX INV CMOS	965-587-60	2	4M,4N
7	IC, 8T97	965-643-01	1	5A
8	IC, 74LS374 OCTAL D LATCH	965-635-05	5	1H-5H
9	IC, 4334-3 1KX4 CMOS RAM	965-613-13	4	2B,2C,2D,2E
10	IC, 74LS86 EXCL-OR	965-635-32	1	5E
11	IC, 74LS04 HEX INV (FC,MO,NL)	965-635-00	4	2A,3A,4A,5D
12	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	1	1A
13	IC, 74LS00 4-2IN NAND (TI)	965-635-07	2	3E,5M
14	IC, 74LS10 3-3IN NAND (TI)	965-635-08	3	4D,4E,4F
15	IC, 74LS30 1-8IN NAND (TI)	965-635-10	1	4B
16	IC, 74LS02 QUAD 2 IN NOR	965-635-17	3	3D,4C,5N
17	IC, 74LS74 DUAL D F/F	965-635-19	4	5B,5K,5L,5F
18	IC, 74LS138 3-8 DEC/MUX	965-635-22	1	3C
19	IC, 74LS27 3-3IN POS-NOR(TI,FC)	965-635-25	1	3B
20	IC, 74LS175 QUAD D F/F	965-635-46	1	5C
21	IC, 74LS244 BUS BUFFER	965-635-03	1	5J
22				
23				
24				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, ALARM BOARD		231-4360-05	B
	MODEL NO. 235	DATE 2-27-80	SHEET 4 OF 5

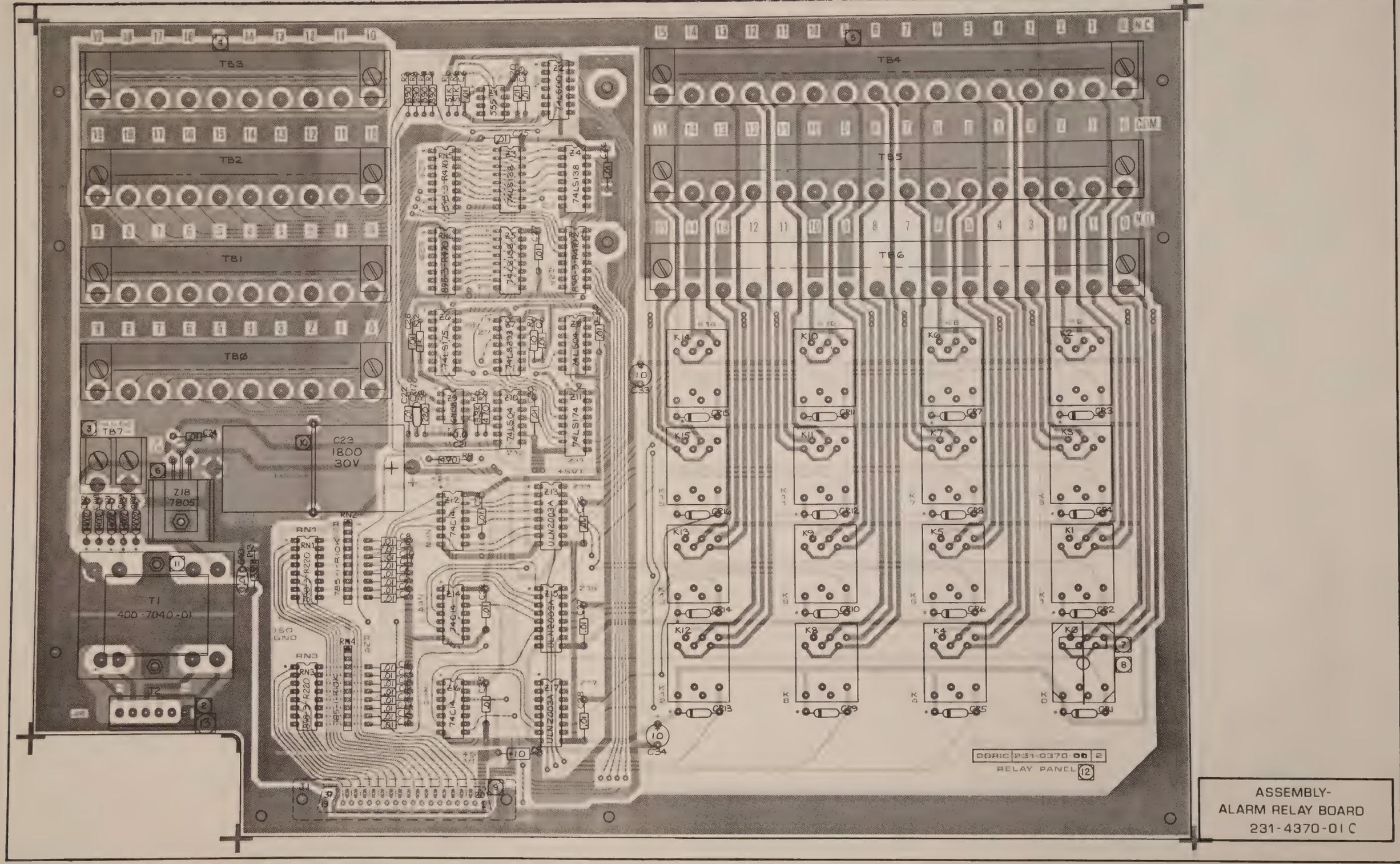
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ±5%, 82	942-208-20	1	R15
26	RES, CARBON 1/4W ±5%, 1K	942-201-02	2	R11,12
27	RES, CARBON 1/4W ±5%, 10K	942-201-03	5	R7-10, R4
28	RES, CARBON 1/4W ±5%, 220	942-202-21	1	R5
29	RES, CARBON 1/4W ±5%, 330K	942-203-34	1	R6
30	RES, CARBON 1/4W ±5%, 680	942-206-81	2	R2,3
31	RES, NETWK 10K SIP (785-1-R10K)	952-010-02	3	RN3,RN2, RN8
32	RES, NTWK, 470 DIP (898-3-R470)	950-047-00	4	RN7,RN4,RN5,RN6
33	RES, CARBON 1/4W ±5%, 3.3K	942-203-32	1	R1
34	RES, NETWK, 1K SIP (785-3-R1K)	952-010-01	1	RN1
35	RES, CARBON 1/4W ±5%, 10K	942-201-03	1	R13
36	RES, CARBON 1/4W ±5%, 390	942-203-91	1	R14
37	RES, CARBON 1/4W ±5%, 150	942-201-51	1	R16
38	CAP, AXIAL .01/50V 180/Z5V050A	900-021-07	18	C3,5,7,9-23
39	CAP, DISC, 100PF @ 1KV (5GA)	901-011-01	3	C1,2,25
40	CAP, TANT, 10 @ 10V	916-010-10	4	C4,6,8,24
41	CAP, DISC .01 @ 500V	900-021-04	1	C26
42				
43				
44	XSTR, 2N2907 (PNP)	962-290-70	1	Q7
45	DIODE, 1N5226	961-522-60	1	CR15
46	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	14	CR1-14
47	XSTR, 2N3646 (NPNSH106)(MO,FC)	962-364-64	2	Q1-2
48	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	2	Q4-5

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, ALARM BOARD	MODEL NO. 235	DATE 2-27-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	1	Q3
50	OPTO ISO-DUAL (LIT-ILCT6)	000-7540-00	22	1KA,B-4KA, B,1LA,B-4LA,B,1M,A,B,-3M,A,B
51	XSTR, PN2222	962-222-20	1	Q6
52	SWITCH, DIP3P (GH76SCO3S)	969-050-17	1	S3
53	SWITCH, ALCO TPA11FG-PC-2	969-050-16	1	S2
54	CHASSIS FASTENER 632B2 US1590B1	991-020-26	1	
55				
56	CONN, PC37 PIN (F)(AMP745108-2)	973-010-78	2	J1,2
57				
58	BATT 2.4V GE41B901BE11G1	975-100-08	1	BT 1 Install at test level
59	SCREW, PAN HD PHILLIPS 4-40 X 3/8 LG	980-440-038	4	J1,2
60	NUT, RADIAL 4-40	984-200-440	4	J1,2
61	WASHER, SPLITLOCK #4	986-200-04	4	J1,2
62	WASHER, FLAT NO. 4	986-100-04	4	J1,J2
63	SCREW PHMS 6-32 X 1/2 LG	980-632-050	1	
64	WASHER, FLAT #6	986-100-06	1	
65	WASHER, SPLITLOCK #6	986-200-06	1	
66				
67				
68				
69				
70				
71				
72				



ASSEMBLY-
ALARM RELAY BOARD
231-4370-01 C

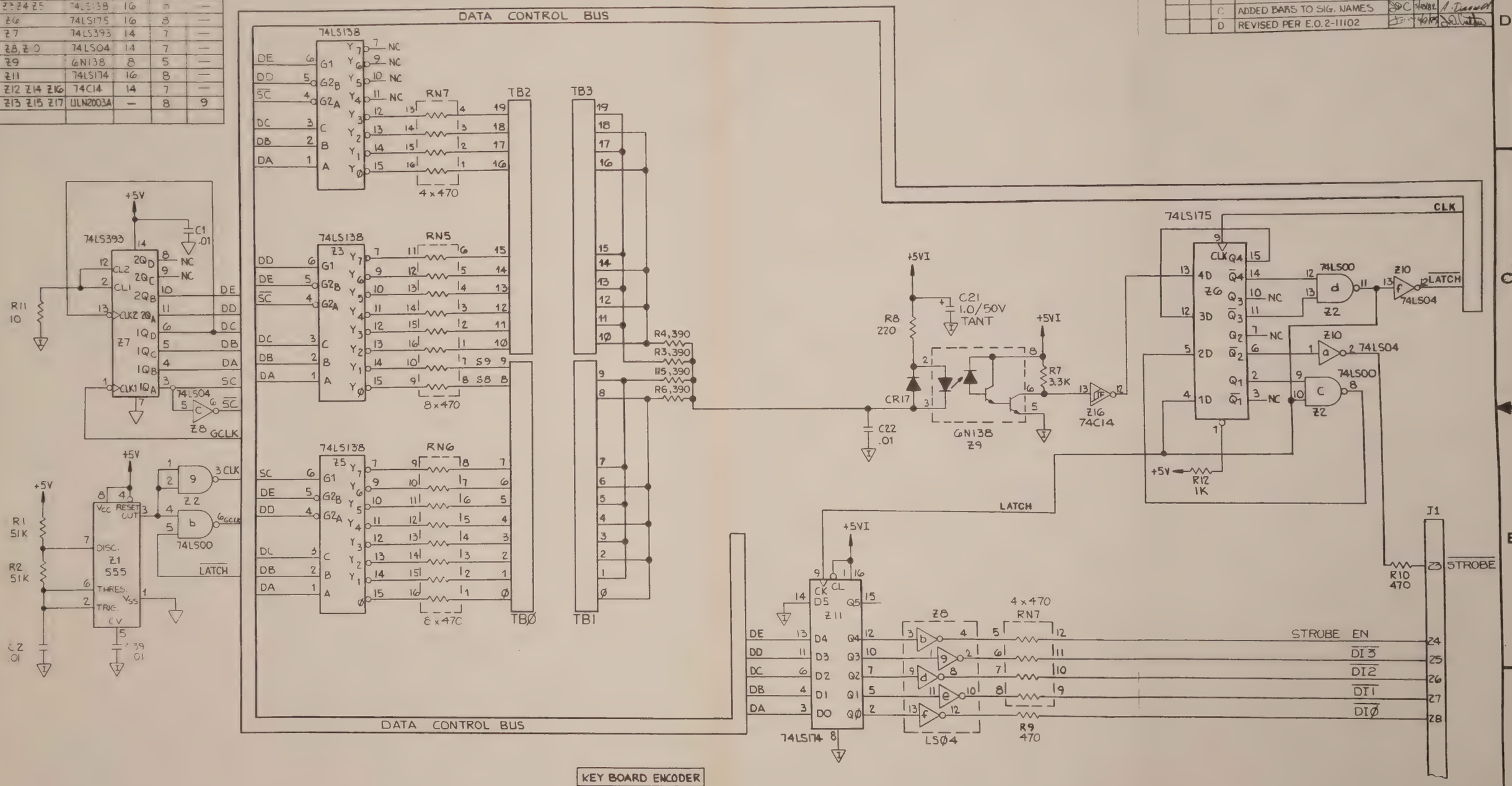
IC POWER DISTRIBUTION TABLE

REF DES	TYPE	+5V	GND	+24V
Z1	555	8	1	—
Z2	74LS00	14	7	—
Z3 Z4 Z5	74LS138	16	8	—
Z6	74LS175	16	8	—
Z7	74LS393	14	7	—
Z8, Z10	74LS04	14	7	—
Z9	6N138	8	5	—
Z11	74LS174	16	8	—
Z12 Z14 Z16	74C14	14	7	—
Z13 Z15 Z17	ULN2003A	—	8	9

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUE IN uF
2. RESISTOR VALUES ARE IN OHMS, 1/4W
3. DIODES ARE IN 914/IN 4148

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A	LIMITED USAGE RELEASE			
		A5	REVISED PER E.O. 2-10226			
		B	PRODUCTION RELEASE PER E.O. 2-10403			
		C	ADDED BARS TO SIG. NAMES			
		D	REVISED PER E.O. 2-11102			



ASSEMBLY NO. 231-4370

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SUPERSEDES

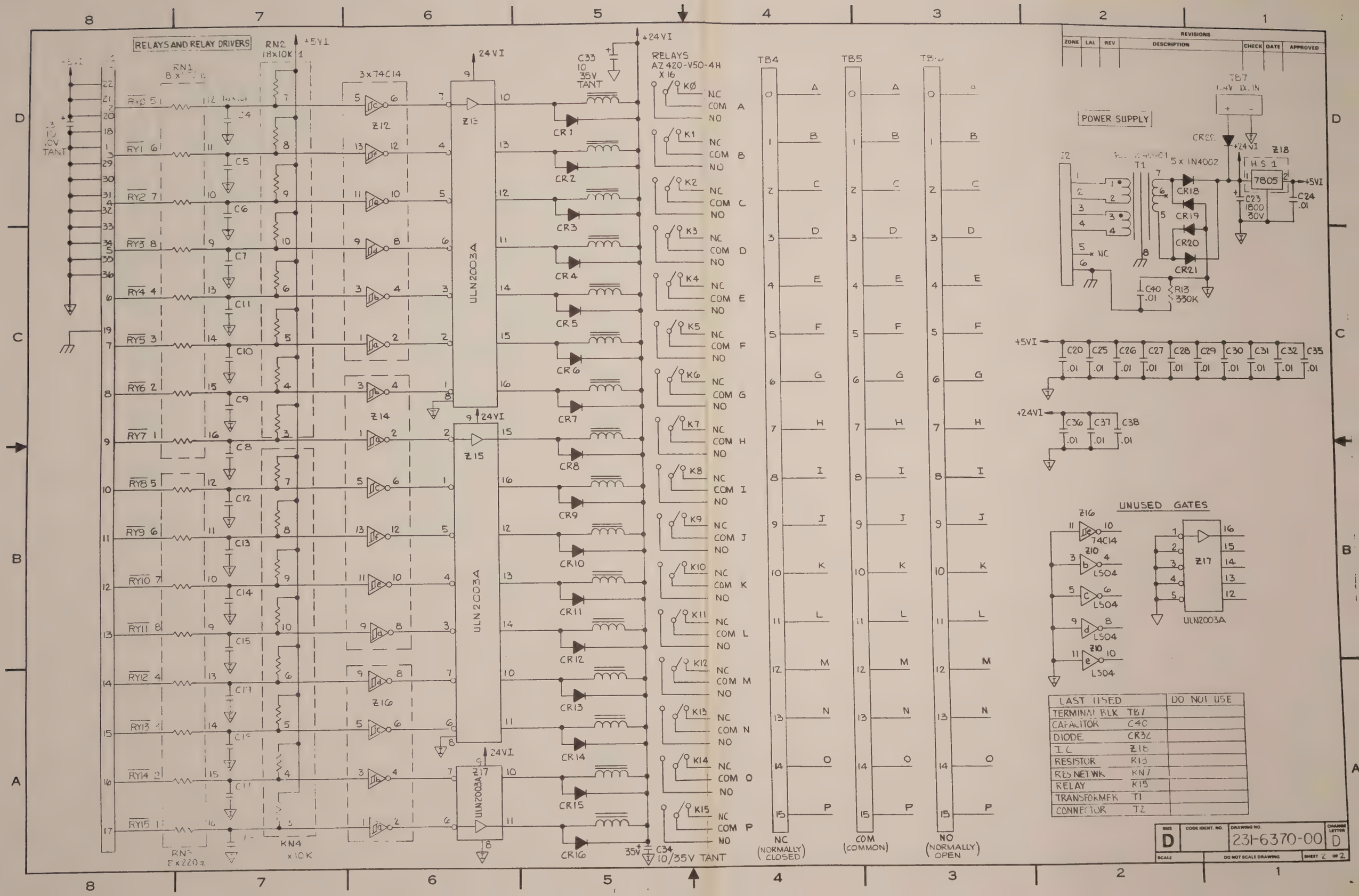
DES/ENG		
DRAWN	GLORIA RUIZ	6-4-80
CHECK		
APPR.		6-17-80

DORIC — DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3800 RUFFIN ROAD • SAN DIEGO, CA 92123

TITLE: SCHEMATIC-RELAY PANEL

SIZE: D — DRAWING NO: 231-6370-00 — CHANGE LETTER: D

SCALE — DO NOT SCALE DRAWING — SHEET 1 OF 2


RELAYS AND RELAY DRIVERS
RN1
RN2 18x10K
+5VI
3x74C14
24VI
ULN2003A
Z12
Z13
Z14
Z15
Z16
Z17
C33 10 35V TANT
+24VI
RELAYS AZ420-V50-4H X16
K0
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
NC
COM
NO
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
RY0 5
RY1 6
RY2 7
RY3 8
RY4 4
RY5 3
RY6 2
RY7 1
RY8 5
RY9 6
RY10 7
RY11 8
RY12 4
RY13 3
RY14 2
RY15 1
RN3 8x220Ω
RN4 x10K
35V C34 10/35V TANT
TB4
TB5
NC (NORMALLY CLOSED)
COM (COMMON)
NO (NORMALLY OPEN)
POWER SUPPLY
TB7
CR22
Z18
HS1
7805
5x1N4002
T1
CR18
CR19
CR20
CR21
C23 1800 30V
C24 .01
C40 .01
R13 330K
C20 C25 C26 C27 C28 C29 C30 C31 C32 C35
C36 C37 C38
UNUSED GATES
Z16 74C14
Z10 LS04
Z17 ULN2003A
REVISIONS
ZONE LAL REV DESCRIPTION CHECK DATE APPROVED
LAST USED DO NOT USE
TERMINAL BLK TB7
CAPACITOR C40
DIODE CR32
IC Z16
RESISTOR R13
RES NET WK RN7
RELAY K15
TRANSFORMER T1
CONNECTOR J2
SIZE D
CODE IDENT. NO.
DRAWING NO. 231-6370-00
CHANGE LETTER D
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 2

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
PCB ASSEMBLY, ALARM RELAY PANEL	MODEL NO. 235	231-4370-01	D
	DATE 4	SHEET 3 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, RELAY PANEL	231-2370-00	1	
2	SCHEMATIC	231-6370-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 555 TIMER	965-586-00	1	Z1
7	IC, 74LS393	965-635-06	1	Z7
8	IC, 74LS138	965-635-22	3	Z3-5
9	IC, 74C14	965-587-60	3	Z12,14,16
10	IC, ULN2003A	965-625-01	3	Z13,15,17
11	IC, 6N138 OPTO	965-570-01	1	Z9
12	IC, 74LS175	965-635-46	1	Z6
13	IC, 74LS00	965-635-07	1	Z2
14	IC, 74LS174	965-635-23	1	Z11
15	IC, 74LS04	965-635-00	2	Z8,Z10
16				
17				
18				
19	RES, CARBON 1/4W ± 5%, 10 Ω	942-201-00	1	R11
20	RES, CARBON 1/4W ± 5%, 1K	942-201-02	1	R12
21	RES, CARBON 1/4W ± 5%, 220	942-202-21	1	R8
22	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	1	R7
23	RES, CARBON 1/4W ± 5%, 390	942-203-91	4	R3··R6
24	RES, CARBON 1/4W ± 5%, 51K	942-205-13	2	R1,R2

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, ALARM RELAY PANEL	MODEL NO. 235	231-4370-01	D
	DATE [illegible]	SHEET 4 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES NTWK SIP 785-1-R10K	952-010-02	2	RN2,RN4
26	RES NTWK DIP 898-3-R220	951-022-00	2	RN1,3
27	RES NTWK DIP 898-3-R470	950-047-00	3	RN5,6,7
28	RES, CARBON 1/4W ±5%, 470	942-204-71	2	R9,R10
29	RES, CARBON 1/4W ±5%, 330K	942-203-34	1	R13
30	CAP .01 UF 50V (1801Z5U050A)	900-021-07	34	C1,2,4-20,22, 24-32,35-38,39
31	CAP 1UF TANT 50V (196D)	916-010-05	1	C21
32	CAP 10UF TANT 35V (196D)	916-010-35	2	C33,C34
33	CAP 1800UF ELECT 30V (39D)	910-180-30	1	C23
34	CAP 10UF TANT 10V (162D)	916-010-10	1	C3
35	CAP, DISC, .01 @ 500V (5GA)	900-021-04	1	C40
36				
37				
38				
39	DIODE 1N4002 100V 1A	966-002-00	5	CR18-22
40	DIODE 1N914 (1N4148)	961-091-40	17	CR1-17
41				
42				
43				
44				
45				
46	REGULATOR, 7805 (5V)	965-551-00	1	Z18
47	HEATSINK, THERMALLOY THM6073	991-008-00	1	
48	XFORMER, POWER 115/230VAC	400-7040-01	1	T1

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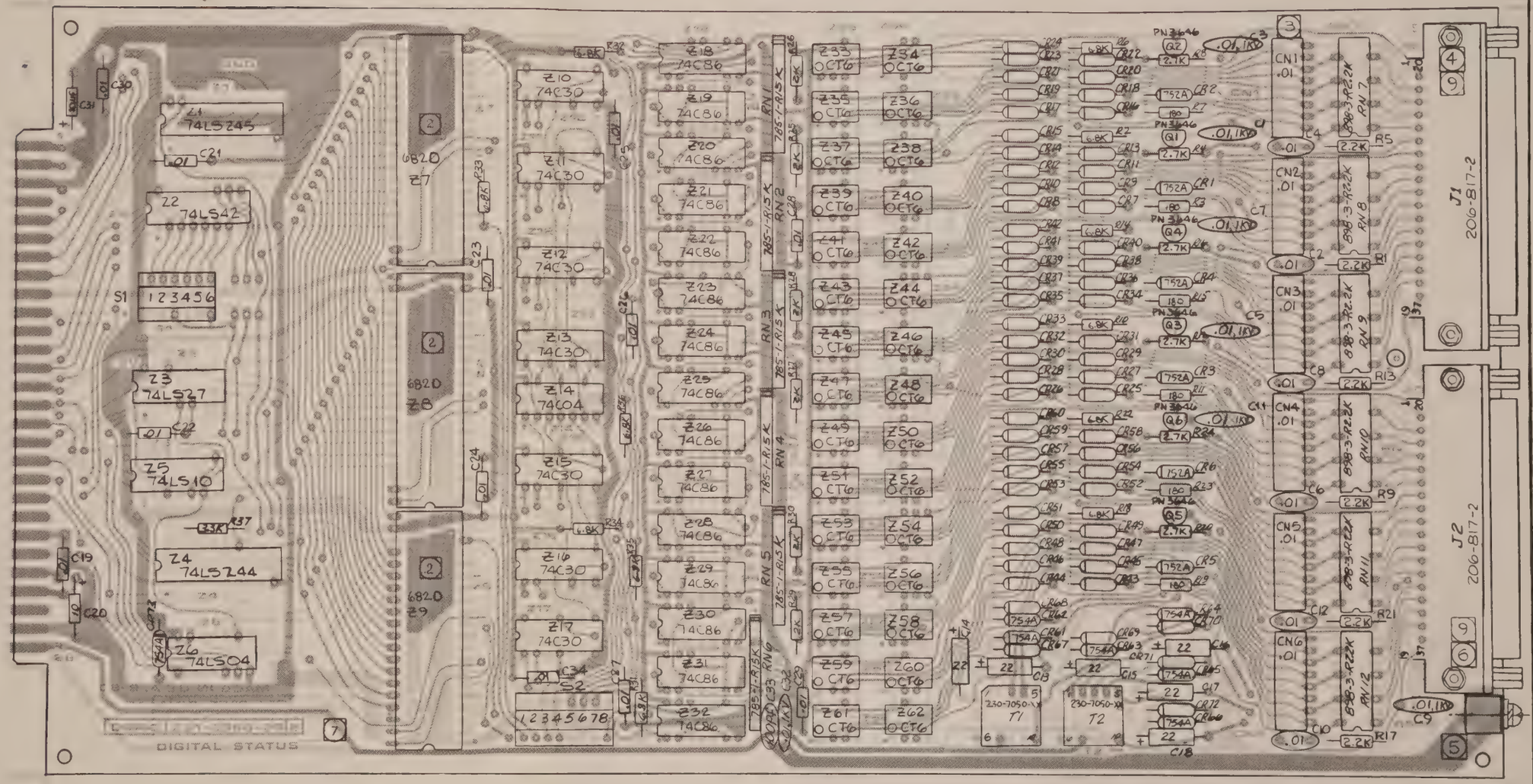
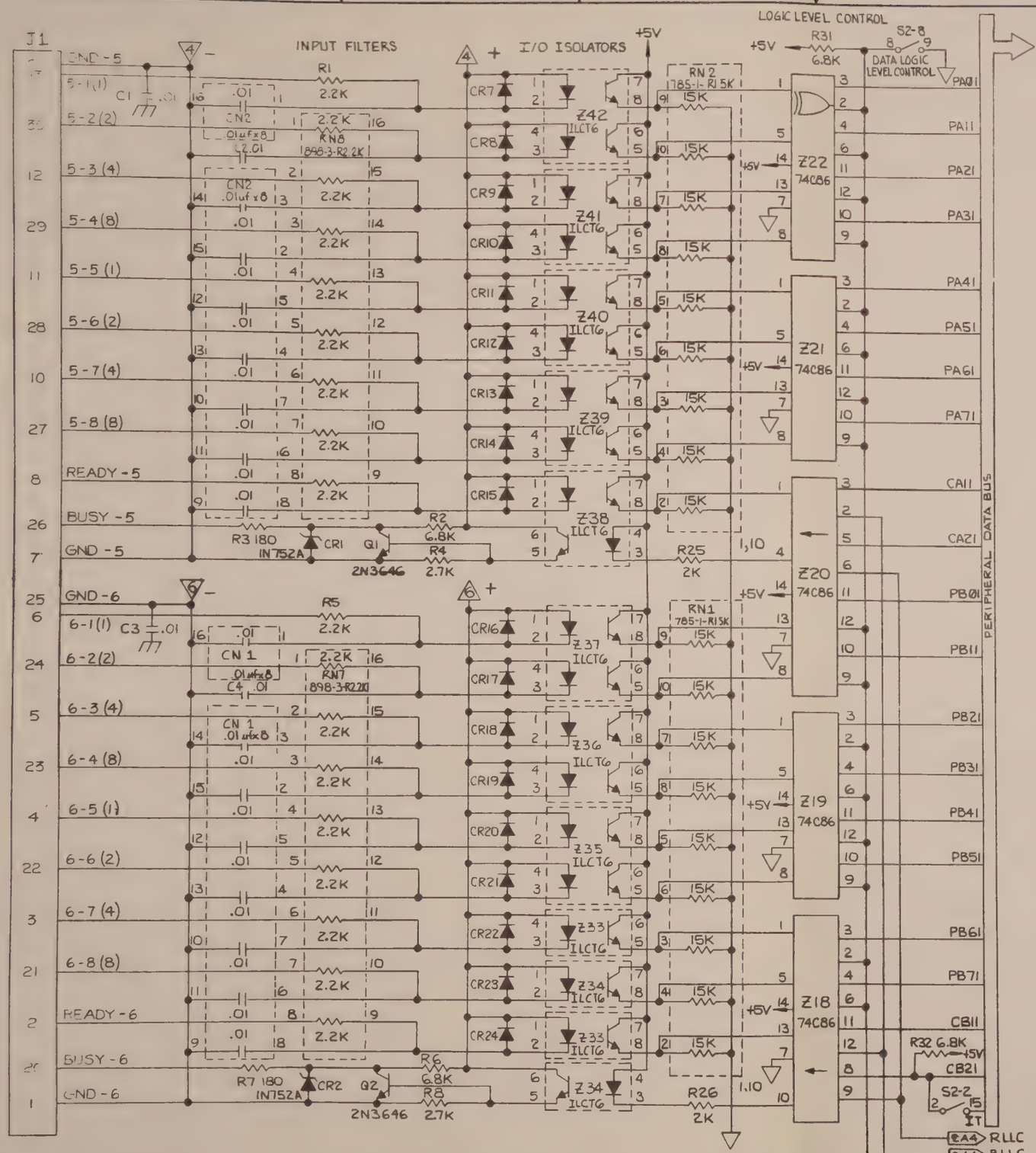
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, ALARM RELAY PANEL	MODEL NO. 235	231-4370-01	D
	DATE 4 5 78	SHEET 5 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RELAYS, AZ420-V50-4H	970-026-00	16	K0-15
50	CONN 37 PIN AMP 205713-2	973-030-03	1	J1
51	SCREWLOCK, FEMALE (AMP 205817-1)	973-010-54	1	
52	RELAY SOCKET (AMZET ST140-A1)	992-010-77	16	
53	RELAY RETAINER (AMZET ST 140-1)	973-010-91	16	
54	TERMINAL BLOCK, 16T (RDI 6PCV16)	973-010-67	3	TB4-TB6
55	TERMINAL BLOCK, 10T (RDI 6PCV10)	973-030-02	4	TB0-TB3
56	TERMINAL BLOCK, 2T (RDI 6PCV02)	973-030-01	1	TB7
57	CONN 6 PIN MOLEX 09-65-1061	973-030-04	1	J2
58	SCREW #6-32 X 5/16	980-632-031	1	
59	SCREW, PAN HD PHILLIPS, 4-40 X 1-1/4" LG	980-440-125	2	
60	WASHER, SPLITLOCK #6	986-200-06	1	
61	FASTENER, SELF LOCKING, TINNERMAN	991-0201-14	2	
62	NUT, RADIAL #6-32	984-200-632	1	
63				



ASSEMBLY
DIGITAL STATUS - I
231 - 4350 - 00 D



NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFIC WORD DESIGNATION AND PIN OUT CAN BE FOUND IN SECTION 3 IN THE OPERATORS MANUAL. (DWG. 231-4000-XX)

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		A	LIMITED USAGE RELEASE			
		A1	LIMITED USAGE RELEASE			
		A6	RELEASED PER E.O. 2-10287			
		B	PRODUCTION RELEASE PER E.O. 2-10403			
		C	REVISED PER E.O. 2-10691			
		D	REVISED PER E.O. 2-10923			

I.C POWER DISTRIBUTION TABLE

REFERENCE DESIG	IC TYPE	POWER +5V	POWER GND
Z1	74LS245	20	10
Z2	74LS42	16	8
Z3	74LS27	14	7
Z4	74LS244	20	10
Z5	74LS10	14	7
Z6	74LS04	14	7
Z7,Z8,Z9	6820	20	1
Z10-Z13 Z15-Z17	74C30	14	7
Z14	74C04	14	7
Z18-Z32	74C86	14	7

LAST USED	DO NOT USE
CAPACITORS C34	
RESISTORS R37	
DIODES CR73	
TRANSISTORS Q6	
SWITCHES S3	
CONNECTORS J2	
RES NET WK. RN12	
CAP. NET. WK. CN6	

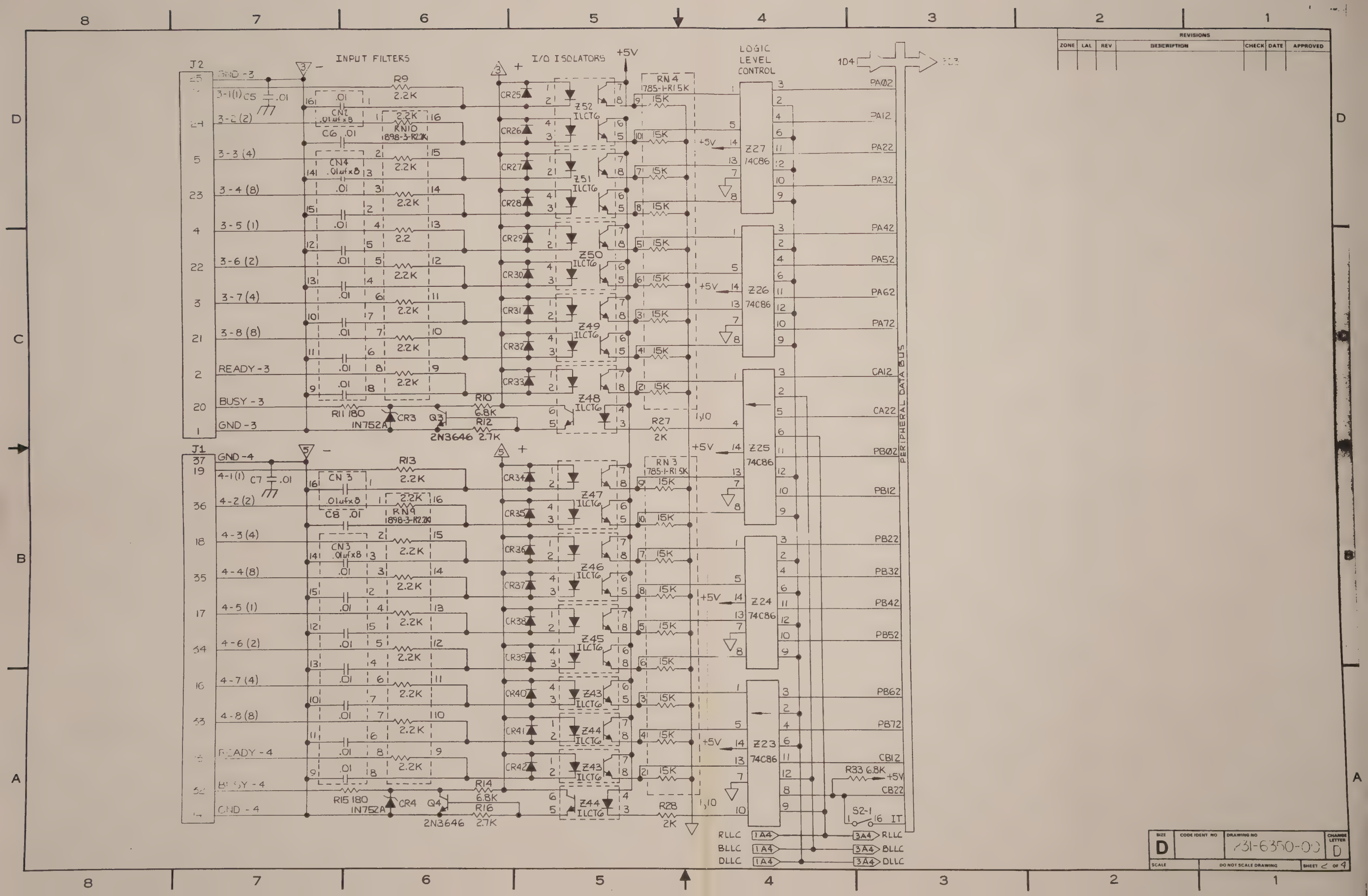
231-4350-XX

DOPIC DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO CA 92123

SCHEMATIC DIGITAL STATUS

SIZE D | DRAWING NO. 231-6350-00 | REV D

SCALE | DO NOT SCALE DRAWING | SHEET 1 OF 4



INPUT FILTERS
I/O ISOLATORS
LOGIC LEVEL CONTROL
PERIPHERAL DATA BUS
J2
J1
GND -3
3-1(1)
3-2 (2)
3-3 (4)
3-4 (8)
3-5 (1)
3-6 (2)
3-7 (4)
3-8 (8)
READY -3
BUSY -3
GND -3
GND -4
4-1(1)
4-2 (2)
4-3 (4)
4-4 (8)
4-5 (1)
4-6 (2)
4-7 (4)
4-8 (8)
READY -4
BUSY -4
GND -4
CN2 .01uf x8
CN4 .01uf x8
CN3 .01uf x8
RN10 1898-3-R2.2K
RN9 1898-3-R2.2K
RN4 785-1-R1.5K
RN3 785-1-R1.5K
Z52 ILCT6
Z51 ILCT6
Z50 ILCT6
Z49 ILCT6
Z48 ILCT6
Z47 ILCT6
Z46 ILCT6
Z45 ILCT6
Z43 ILCT6
Z44 ILCT6
Z27 74C86
Z26 74C86
Z25 74C86
Z24 74C86
Z23 74C86
R9 2.2K
R10 6.8K
R11 180
R12 2.7K
R13 2.2K
R14 6.8K
R15 180
R16 2.7K
R27 2K
R28 2K
R33 6.8K
CR3 1N752A
CR4 1N752A
Q3 2N3646
Q4 2N3646
S2-1
IT
PA02
PA12
PA22
PA32
PA42
PA52
PA62
PA72
CA12
CA22
PB02
PB12
PB22
PB32
PB42
PB52
PB62
PB72
CB12
CB22
RLLC
BLLC
DLLC
1A4
3A4
REVISIONS
ZONE
LAL
REV
DESCRIPTION
CHECK
DATE
APPROVED
SIZE
D
CODE IDENT NO
DRAWING NO
231-6350-00
CHANGE LETTER
D
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 4

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

INPUT FILTERS

I/O ISOLATORS

LOGIC LEVEL CONTROL

+5V

J2

GND - 1
1-1 (1)
1-2 (2)
1-3 (4)
1-4 (8)
1-5 (1)
1-6 (2)
1-7 (4)
1-8 (8)
READY - 1
BUSY - 1
GND - 1
GND - 2
2-1 (1)
2-2 (2)
2-3 (4)
2-4 (8)
2-5 (1)
2-6 (2)
2-7 (4)
2-8 (8)
READY - 2
BUSY - 2
GND - 2

C9 .01
C10 .01
C11 .01
C12 .01
CN4 .01μf x8
CN5 .01μf x8
CN6 .01μf x8
RN12 898-3-R2.2K
RN11 898-3-R2.2K
R17 2.2K
R18 6.8K
R19 180
R20 2.7K
R21 2.2K
R22 6.8K
R23 180
R24 2.7K
R29 2K
R30 2K
R34 6.8K
R35 6.8K
R36 6.8K
CR5 IN752A
CR6 IN752A
Q5 2N3646
Q6 2N3646
CR43 CR44 CR45 CR46 CR47 CR48 CR49 CR50 CR51 CR52 CR53 CR54 CR55 CR56 CR57 CR58 CR59 CR60
Z62 Z61 Z60 Z59 Z58 Z57 Z56 Z55 Z54 Z53 ILCT6
RN6 785-1-R15K
RN5 785-1-R15K
15K
Z32 Z31 Z30 Z29 Z28 74C86

2D3 4D7

PA03 PA13 PA23 PA33 PA43 PA53 PA63 PA73
CA13 CA23
PB03 PB13 PB23 PB33 PB43 PB53 PB63 PB73
CB13 CB23

PERIPHERAL DATA BUS

S2
EVENTS MODE SELECT
SPARE
EVENTS TRIGGER
BCD MODE SELECT
STATUS / EVENTS MODE SELECT
NEG. BUSY
NEG. READY
NEG. DATA

S2-4 S2-3 ET S2-5 IT

READY LOGIC LEVEL CONTROL
S2-7
S2-6
BUSY LOGIC LEVEL CONTROL

RLLC 2A4
BLLC 2A4
DLLC 2A4

SIZE	CODE IDENT NO	DRAWING NO.	CHANGE LETTER
D		231-6350-00	D
SCALE	DO NOT SCALE DRAWING	SHEET 3 OF 4	

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, DIGITAL INPUT BOARD	MODEL NO. 235	DATE 2-28-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB DIGITAL INPUT	231-2350-00	1	
2	SCHEMATIC	231-6350-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	1	Z1
7	IC, 74LS42 BCD-DEC DECODER	965-635-20	1	Z2
8	IC, 74LS27 3-3IN POS-NOR(TI,FC	965-635-25	1	Z3
9	IC, 74LS244 8 3-ST DRV(AMD, SIG	965-635-03	1	Z4
10	IC, 74LS10 3-3IN NAND (TI)	965-635-08	1	Z5
11	IC, 74LS04 HEX INV(FC,MO,NL)	965-635-00	1	Z6
12	IC, MC6820 PIA (MOT)(CERAMIC)	965-613-03	3	Z7,8,9
13	IC, 74C30 1-8IN NAND CMOS	965-587-42	7	Z10-13,15-17
14	IC, 74C04(4069)HEX INV CMOS(RC	965-587-05	1	Z14
15	IC, 74C86 4-2IN EXLU OR(CMOS)	965-565-05	15	Z18-32
16				
17				
18				
19				
20				
21				
22				
23	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	6	R1,5,9,13,17, 21
24	RES, CARBON 1/4W ± 5%, 6.8K	942-206-82	12	R31-36,R2,R6, R10,R14,R18,R22

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, DIGITAL INPUT BOARD	MODEL NO. 235	231-4350-00	D
		DATE 2-28-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ± 5%, 180	942-201-81	6	R3,R7,R11,R15, R19,R23
26	RES, CARBON 1/4W ± 5%, 2.7K	942-202-72	6	R4,R8,R12,R16 R20,R24
27	RES, CARBON 1/4W ± 5%, 2K	942-202-02	6	R25-30
28	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	1	R37
29	RES, NTWRK, 15K SIP 785-1-R15K	951-015-02	6	RN1-6
30	RES NTWK, 16PDIP 898-3,R2.2K	951-022-01	6	RN7-12
31				
32				
33				
34				
35	CAP, DISC .01 @ 1KV (5GA-S10)	900-021-05	7	C32 C1,3,5,7,9,11
36	CAP, DISC, .01 @ 500V (5GA)	900-021-04	6	C2,4,6,8,10,12
37	CAP, TANT 22MF @ 10V (162D)	916-022-10	6	C13-18
38	CAP, TANT 10 @ 10V (162D)	916-010-10	2	C20,C31
39	CAP, DISC, 100PF @ 1KV (5GA)	901-011-01	1	C33
40	CAP, AXIAL .01/50V 1801Z5U050A	900-021-07	12	C21-C30, C19, C34
41	CAP NTWRK, .01uF 926CZ5U103M050B	903-100-00	6	CN1-CN6
42				
43				
44	DIODE, ZENER 1N752A (5.6V)	961-075-21	6	CR1-6
45	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	60	CR7-60 CR68-72
46	DIODE, 1N754A (6.8V) (TD,MO)	961-075-41	7	CR61-66,CR73
47				
48				

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, DIGITAL INPUT BOARD	MODEL NO. 235	DATE 2-28-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	SCREW, PHMS 6-32 X 1/2 LG	980-632-050	1	
50	WASHER, FLAT #6	986-100-06	1	
51	WASHER, SPLITLOCK #6	986-200-06	1	
52	XSTR 3646	962-364-60	6	Q1-Q6
53	SWITCH, DIP-6P1T (GH76SB06S)	969-050-13	1	S1
54	SWITCH, DIP-8PIT (GH76SB08S)	969-050-11	1	S2
55	XFMR, ISOLATION	230-7050-00	2	T1,T2
56	OPTO ISO, DUAL(LIT ILCT6-XXX)	000-7540-00	30	Z33-Z62
57	CONN, PC 37 PIN(F) (AMP745108-2)	973-010-78	2	J1,J2
58	CHASSIS FASTENER, 632B2 (US1590B1)	991-020-26	1	
59				
60	SCREW PHMS 4-40 X 3/8 LG	980-440-038	4	J1,J2
61	NUT RADIAL 4-40	984-200-440	4	J1,J2
62	CABLE ASSY, DIGITAL STATUS (J1)	231-5460-00	1	
63	CABLE ASSY, DIGITAL STATUS (J2)	231-5470-00	1	
64	WASHER SPLIT-LOCK #4	986-200-04	4	J1,J2
65	WASHER, FLAT NO. 4	986-100-04	4	J1,J2
66				
67				
68				
69				
70				
71				
72				

5 INSTALL 40 PIN I.C. SOCKET, (ITEM 94), 1 PLACE.

6 INSTALL CONN, (ITEM 82), TO PCB WITH 4-40 SCREWS, (ITEM 85), NO. 4 FLAT WASHER, (ITEM 88), NO. 4 SPLITLOCK WASHER, (ITEM 90), NUT 4-40, (ITEM 87), SCREW HEAD TO BE ON FAR (CIRCUIT) SIDE OF BOARD.

7 RUBBER STAMP ASSEMBLY NO. [illegible] HIGH [illegible] PERMANENT [illegible] FAR (CIRCUIT) SIDE.

8 FOR MATERIAL LIST, SEE [illegible]

9 INSTALL I.C. (ITEM 27) INTO BOTTOM OF I.C. SOCKET AS SHOWN (4 TOP PINS NOT USED).

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS UNIT TO BE ASSEMBLED TO DORIC SPEC 000-1003.

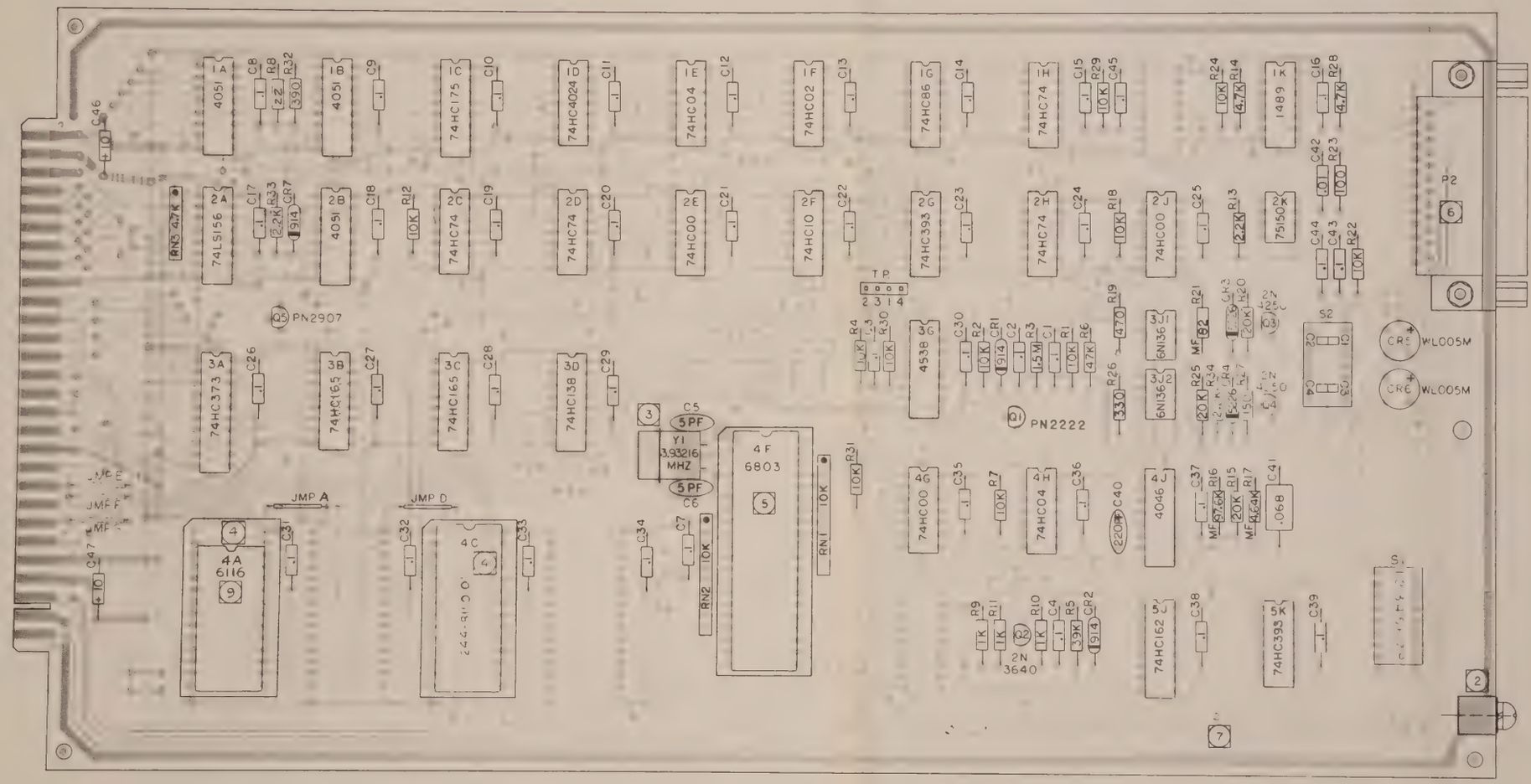
2 INSTALL CHASSIS FASTENER, (ITEM 93), ON COMPONENT SIDE AS SHOWN; AND INSTALL SCREW NO. 6-32 (ITEM 86), NO. 6 SPLITLOCK WASHER, (ITEM 91), AND NO. 6 FLAT WASHER (ITEM [illegible]).

3 INSTALL [illegible]

4 INSTALL 28 PIN I.C. SOCKET, (ITEM 95), 2 PLACES.

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X3	R & D RELEASE	[illegible]	[illegible]	[illegible]
		A1	LTD USAGE REL PER E.O. 2-11431	[illegible]	[illegible]	[illegible]
		E	PROD. REL. PER E.O. 2-11453	[illegible]	[illegible]	[illegible]
		C	REVISED PER E.O. 2-11527	[illegible]	[illegible]	[illegible]
		B	REVISED PER E.O. 2-11585	[illegible]	[illegible]	[illegible]
		[illegible]	REVISED PER E.O. 2-11579	[illegible]	[illegible]	[illegible]
		B	REVISED PER E.O. 2-11619	[illegible]	[illegible]	[illegible]



HOLE TOLERANCES	NOTES UNLESS SPECIFIED	DRAWN	CHECK	APPR
000 250 DIA + 004 002 251 500 DIA + 006 002 501 1 00 DIA + 010 005	1 TOLERANCES XX ± .03 DIMENSIONED ANGLES XXX ± .010 ±1/2° 2 BREAK ALL SHARP EDGES .010 APPROX 3 MACH SURFACES 4 ALL DIM IN INCHES 5 ALL TRUE POSITION TOLERANCES APPLY AT MMC	[illegible]	[illegible]	[illegible]
SUPERSEDES		MATERIAL		
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF DORIC SCIENTIFIC	USED ON: 245S NEXT ASSY 244-0000-XX	FINISH		

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO

TITLE: ASSEMBLY, PCB, SATELLITE CONTROLLER

SIZE	CODE IDENT NO	DRAWING NO	CHANGE LETTER
D		244-4310-01	B

SCALE 2:1 | DO NOT SCALE DRAWING | SHEET 1 OF 6

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED
		X4	R & D RELEASE			
		A1	LTD USAGE REL PER E.O. 2-11431			
		B	PROD. REL. PER E.O. 2-11453			
		b	REVISED PER E.O. 2-11585			
		B	REVISED PER E.O. 2-11619			

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. DIODES ARE 1N914 OR 1N4148.

REF DESIGNATORS	
LAST USED	DO NOT USE
RESISTOR R34	
CAPACITOR C47	
R. NETWORK RN3	
TRANSISTOR Q5	
IC 5K	1J, 5G
CONN P2	
DIODE CR7	
CRYSTAL Y1	
TEST POINT TP4	

COUNTER SYNC GENERATOR

SYNC RESET

WATCH DOG

PARTIAL ADDRESS DECODER

ADDRESS BUS

DATA BUS

OPTIONAL MEMORY

MPU 6803 4F

ASSEMBLY NO 244-4310-XX

SUPERSEDES

DES/ENG PWS

DRAWN

CHECK DWS

APPR.

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TITLE SCHEM., SATELLITE CONTROLLER

SIZE D | DRAWING NO. 214-6310-02 | CHANGE LETTER B

SCALE — | DO NOT SCALE DRAWING | SHEET 1 OF 2

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

FEM SERIAL ENCODER

FEM DATA TRANSMITTER/RECEIVER

SHIFT REGISTER ADDRESS DECODER

SERIAL CLOCK GEN.

SERIAL I/O

UNUSED

P1 (MOTHER BD)

P2

SIZE	CODE IDENT. NO.	DRAWING NO.	CHANGE LETTER
D		244-6310-02	B
SCALE ——	DO NOT SCALE DRAWING	SHEET 2 OF 2	

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO	REV
ASSEMBLY, PCB, SATELLITE CONTROLLER	MODEL NO. 245S	244-4310-02	B
		DATE 10-13-83	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, SATELLITE CONTROLLER	244-2310-02	1	
2	SCHEMATIC, SATELLITE CONTROLLER	244-6310-02	1	
3	TEST SPEC	244-8310-00	REF	
4				
5				
6	IC, 6N136	965-570-09	2	3J1,3J2
7	IC, 1489	965-601-00	1	1K
8	IC, 74LS156	965-635-48	1	2A
9	IC, DS75150J-8	965-642-00	1	2K
10	IC, 74HC00 4-2 IN NAND (TI)	965-6351-00	3	2E,2J,4G
11	IC, 74HC373	965-6351-02	1	3A
12	IC, 74HC02	965-6351-04	1	1F
13	IC, 74HC04	965-6351-05	2	1E,4H
14	IC, 74HC10	965-6351-07	1	2F
15	IC, 74HC74	965-6351-08	4	1H,2C,2D,2H
16	IC, 74HC86	965-6351-09	1	1G
17	IC, 74HC138	965-6351-11	1	3D
18	IC, 74HC162	965-6351-13	1	5J
19	IC, 74HC165	965-6351-14	2	3B,3C
20	IC, 74HC175	965-6351-15	1	1C
21	IC, 74HC393	965-6351-17	2	2G,5K
22	IC, 74HC4024	965-6351-19	1	1D
23	IC, 4046	965-5870-86	1	4J
24	IC, 4051	965-587-77	3	1A,1B,2B

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, SATELLITE CONTROLLER		244-4310-02	B
	MODEL NO. 245S	DATE 10-13-83	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	IC, 4538	965-587-72	1	3G
26	IC, 244 FIRMWARE	244-8150-01	1	4C
27	IC, 6116	965-613-16	1	4A
28	IC, 6803 P1 MICROY 1.25 MHz	965-5590-06	1	4F
29				
30				
31				
32				
33				
34	RES, NETWK, 10K 785-1-R10K	952-010-02	2	RN1,RN2
35	RES, NETWK, 4.7K 783-1-R4.7K	953-047-01	1	RN3
36	RES, FILM RN55C, ±1%, 82	924-308-20	1	R21
37	RES, FILM RN55D, ±1%, 4.64K	924-346-41	1	R17
38	RES, FILM RN55D, ±1%, 97.6K	924-397-62	1	R16
39	RES, CARBON, 1/4W ±5%, 100	942-201-01	1	R23
40	RES, CARBON, 1/4W ±5%, 1K	942-201-02	3	R9,R10,R11
41	RES, CARBON, 1/4W ±5%, 10K	942-201-03	11	R1,R2,R4,R7,R12 R18,R22,R24,R29 R30,R31
42	RES, CARBON, 1/4W ±5%, 150	942-201-51	1	R27
43	RES, CARBON, 1/4W ±5%, 1.5M	942-201-55	1	R3
44	RES, CARBON, 1/4W ±5%, 20K	942-202-03	3	R15,R20,R25
45	RES, CARBON, 1/4W ±5%, 2.2K	942-202-22	3	R13,R33,R34
46	RES, CARBON, 1/4W ±5%, 330	942-203-31	1	R26
47	RES, CARBON, 1/4W ±5%, 39K	942-203-93	1	R5
48	RES, CARBON, 1/4W ±5%, 4.7K	942-204-72	2	R14,R28

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, SATELLITE CONTROLLER	MODEL NO. 245S	244-4310-02	B
		DATE 10-13-83	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON, 1/4W ±5%, 47K	942-204-73	1	R6
50	RES, CARBON, 1/4W ±5%, 22	942-202-20	1	R8
51	RES, CARBON, 1/4W ±5%, 390	942-203-91	1	R32
52	RES, CARBON, 1/4W ±5%, 470	942-204-71	1	R19
53				
54				
55				
56	CAP, .01µf/50V	900-021-07	1	C42
57	CAP, .1µf/50V	900-021-08	40	C1-C4,C7-C39, C43-C45
58	CAP, POLYCARB, .068µf	911-036-83	1	C41
59	CAP, MICA, 5pf	915-030-50	2	C5,C6
60	CAP, MICA, 220pf	915-032-21	1	C40
61	CAP, TANT, 10µf/10V	916-010-10	2	C46,C47
62				
63				
64				
65				
66				
67	DIODE, 1N914	961-091-40	3	CR1,CR2,CR7
68	DIODE, ZENER 1N5226, 3.3V	961-522-60	2	CR3,CR4
69				
70				
71				
72				

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MATERIAL LIST

DRAWING TITLE		DRAWING NO.	REV
ASSEMBLY, PCB, SATELLITE CONTROLLER	ML	244-4310-02	B
	MODEL NO. 245S	DATE 10-13-83	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74	XSTR, PN2907	962-290-70	1	Q5
75	XSTR, PN2222	962-222-20	1	Q1
76	XSTR, 2N3640	962-364-00	1	Q2
77	XSTR, 2N4250	962-425-00	2	Q3,Q4
78	RECTIFIER BRIDGE, WL005M	966-002-26	2	CR5,CR6
79	XTAL, 3.93216 MHZ, HC18	967-005-12	1	Y1
80	SWITCH, DIP 8P1T	969-050-11	1	S1
81	SWITCH, DIP 2P2T	969-050-15	1	S2
82	CONN, RECEPT 25 PIN	973-010-75	1	P2
83	CONN, 4 PIN HEADER	973-3700-14	1	TP1-TP4
84				
85	SCREW, PAN HD PHILLIPS, 4-40 X 3/8 LG	980-440-038	2	(P2)
86	SCREW, PAN HD PHILLIPS, 6-32 X 1/2 LG	980-632-050	1	
87	NUT, RADIAL 4-40	984-200-440	2	(P2)
88	WASHER, FLAT #4	986-100-04	2	(P2)
89	WASHER, FLAT #6	986-100-06	1	
90	WASHER, SPLITLOCK #4	986-200-04	2	(P2)
91	WASHER, SPLITLOCK #6	986-200-06	1	
92	JUMPER, .500 X .125	991-010-05	5	JMP A-B,JMP C-D JMP E,JMP F,JMP G
93	CHASSIS FASTENER, 6-32	991-020-26	1	
94	SOCKET, IC, 40 PIN	992-010-18	1	(4F)
95	SOCKET, IC, 28 PIN	992-010-85	2	(4A,4C)
96				